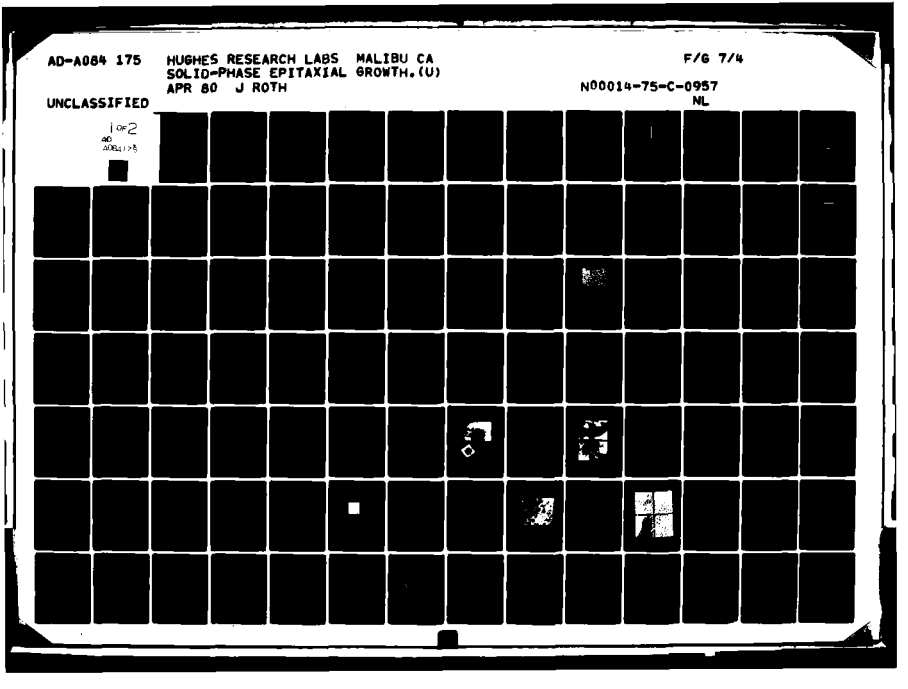
AD-A084 175 HUGHES RESEARCH LABS MALIBU CA F/G 7/4
SOLID-PHASE EPITAXIAL GROWTH.(U)
APR 80 J ROTH N00014-75-C-0957
UNCLASSIFIED NL



SOLID–PHASE EPITAXIAL GROWTH

John Roth

Hughes Research Laboratories

3011 Malibu Canyon Road

Malibu, CA 90265

April 1980

N00014–75–C–0957

Final Report

1 May 1975 through 30 June 1979

Approved for public release; distribution unlimited.

Sponsored by

OFFICE OF NAVAL RESEARCH

DEPARTMENT OF THE NAVY

800 N. Quincy Street

Arlington, Virginia 22217

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A084 175	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) SOLID-PHASE EPITAXIAL GROWTH		5. TYPE OF REPORT & PERIOD COVERED Final Report 1 May 1975-30 June 1979
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) John Roth		8. CONTRACT OR GRANT NUMBER(s) N00014-75-C-0957
9. PERFORMING ORGANIZATION NAME AND ADDRESS Hughes Research Laboratories 3011 Malibu Canyon Road Malibu, California 90265		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research Department of the Navy 800 N. Quincy St., Arlington, Virginia 22217		12. REPORT DATE April 1980
		13. NUMBER OF PAGES 107
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Silicon, Epitaxy, Silicides, Thin films, Ultrahigh vacuum.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

We report on the growth of Si single-crystal films by solid-phase epitaxy (SPE). Two variants of SPE are discussed: (1) direct SPE, in which an amorphous Si film is deposited onto a clean single-crystal substrate then heated to cause epitaxial crystallization, and (2) silicide-interlayer SPE, in which a thin transition-metal film is deposited onto the substrate and reacted with it prior to the deposition of amorphous Si to scavenge surface contaminants and permit epitaxy.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

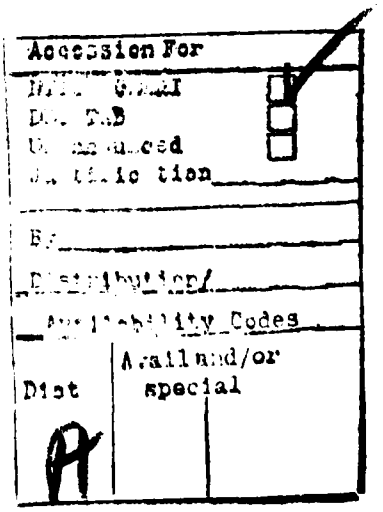
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

We show that previous work on silicide-interlayer SPE was dominated by contaminant effects and did not represent the intrinsic behavior of the process. Surprisingly, however, conducting interlayer SPE in a noncontaminating, ultrahigh vacuum (UHV) environment did not improve the quality of the films, but instead changed the growth morphology, with the result that even films grown under the most stringent vacuum conditions are unsuitable for most microelectronic applications. It appears that certain foreign contaminants may actually be ncessary in silicide-interlayer SPE to hold the silicide together during Si transport.

The direct SPE of Si deposited onto a clean substrate is shown to produce high-quality epitaxial films on Si <100> . MOS transistors fabricated in SPE layers grown at 550°C functioned identically to their bulk Si counterparts, demonstrating the suitability of SPE for device applications. Dopants introduced during film deposition are activated with high efficiency during SPE growth. Also, neither film nor substrate dopants diffuse measurably during growth at 550°C, thus permitting arbitrary doping profiles to be produced. The crystallographic quality of SPE films is shown to be relatively independent of growth temperature and film thickness provided that the introduction of contaminants is strictly avoided.

Several sources of contaminant introduction in SPE are discussed, and their effects on the growth morphology and crystal quality are reported. A Si cleaning procedure is reported that produces surfaces having less than one monolayer of adsorbed O and C. However, films grown on even slightly contaminated substrates are found to have high defect densities. We present Auger spectroscopy depth profiles which show that UHV-deposited amorphous Si films absorb large quantities of O and C when exposed to room air. One manifestation of this contaminant absorption is that a polycrystalline surface layer forms on SPE samples exposed to room air prior to growth. Poly formation in SPE of air-exposed samples can be minimized by using low growth temperatures and/or very thin films, but the absorption of O and C to concentrations of $10^{18}/cm^3$ and above can probably only be avoided by using all-UHV processing.

TABLE OF CONTENTS



LIST OF ILLUSTRATIONS

SECTION 1

INTRODUCTION

During the solid-phase epitaxy (SPE) process, an amorphous solid film is converted to an epitaxial single crystal layer by heating to a temperature less than the melting point of the film. This report deals exclusively with the amorphous-to-single-crystal conversion of deposited semiconductor films, although SPE can occur in other circumstances, notably in the recrystallization of the surface of a crystal made amorphous by ion-implantation damage. Much of the large body of data accumulated from studies of SPE in implanted layers applies equally well to deposited films. In a practical sense, however, studies of SPE in deposited films entail some complications that are not present in the implant work. Foremost among these is the susceptibility of a deposited amorphous film to contaminant absorption during exposure of the film to room air. This effect makes it difficult to determine the intrinsic behavior of SPE in a deposited film unless all the measurements are conducted in a noncontaminating ambient. Consequently, most of our experimental work involved the use of ultrahigh vacuum (UHV) processing to avoid contaminant effects.

SPE differs from other forms of epitaxy, such as liquid-phase epitaxy (LPE) and vapor-phase epitaxy (VPE), in that the physical state of the medium which supplies atoms to the growing epitaxial layer is a solid film instead of a liquid (LPE) or vapor (VPE). This basic difference between the three forms of epitaxy is depicted in Figure 1. In addition to physical differences between LPE, VPE, and SPE, they also differ significantly in the temperatures used during growth. LPE of Si is conducted at temperatures just below the melting point, which for Si is about 1415°C, and VPE is usually conducted in the 900 to 1100°C range. In comparison, SPE growth occurs at reasonable rates at temperatures of only 500 to 600°C.

The possibility of growing epitaxial semiconductor films at such low temperatures has important technological implications: epitaxial films can be grown without disturbing either the distribution of

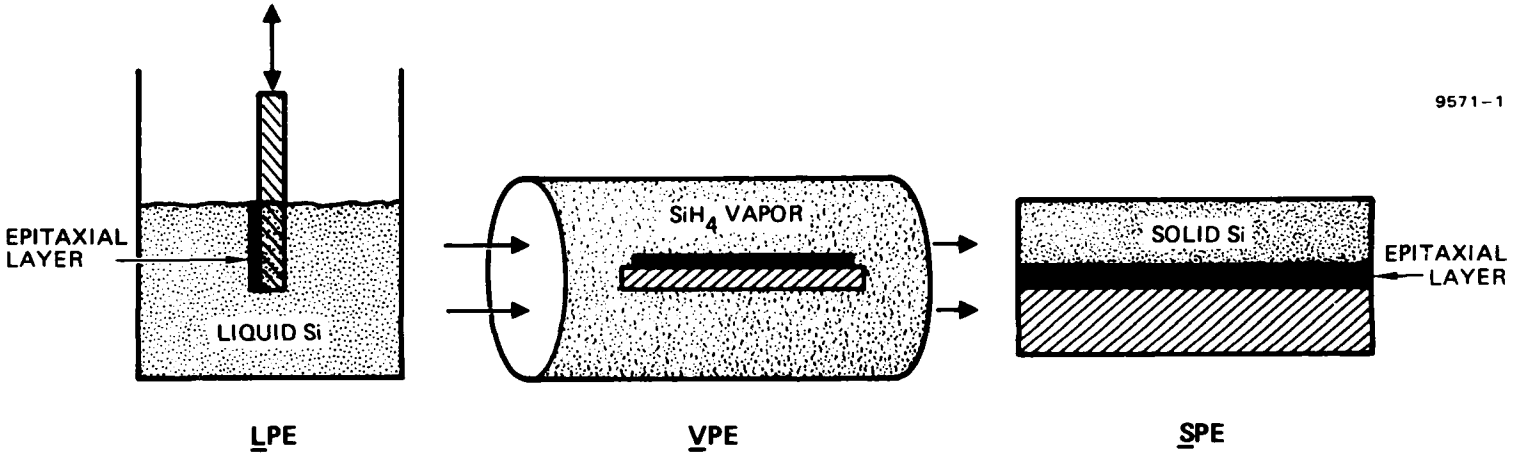


Figure 1. Comparison of Si growth by liquid-phase (LPE), vapor-phase (VPE), and solid-phase (SPE) epitaxy. In each case, the cross-hatched region is the single-crystal substrate, the dotted region is the source of Si, and the shaded region is the epitaxial film.

dopant atoms present in the substrate or doping profiles within the epitaxial film itself. The doping can be arbitrarily tailored since diffusive redistribution of dopants during growth is negligible. This characteristic of SPE makes it attractive for the fabrication of high-frequency devices and very-large-scale integrated circuits. In addition to its technological importance, SPE embodies several mechanisms of fundamental importance to our understanding of solid materials and their interactions.

The thermodynamic basis for the occurence of SPE is as follows. An amporphous semiconductor film is not in a state of minimum free energy and therefore is at best metastable. This is especially true for films of covalently bonded solids since a high density of unsaturated chemical bonds raises the enthalpy of the system while a lack of long-range order causes the entropy to be minimum. Consequently, the free energy of an amorphous film can be lowered by crystallization. Even an isolated piece of amorphous Si would eventually crystallize at non-zero temperature. However, as depicted in Figure 2, a heated chunk of Si would not immediately become a single crystal since the crystallization process starts simultaneously at many random locations. The result would instead be a "polycrystalline" solid consisting of many individual, randomly oriented "grains."

The polycrystalline state, however, is not the state of lowest possible free energy because of the excess energy of unsaturated bonds at the boundaries between individual crystal "grains" and the lack of long-range order. Therefore, one grain will eventually grow at the expense of the others in order to progress toward the lowest free energy state. As suggested in Figure 2, this final conversion would probably take a very long time in an isolated piece of Si. This raises the second important consideration in SPE: the necessity of providing a kinetically favorable path directly from the amorphous initial state to the single-crystal final state. In practical terms, this can be accomplished by ensuring that the amorphous solid is in intimate contact with a single-crystal "seed" which serves as a template for the crystallization process. When such a seed is present, epitaxial single-crystal growth proceeds from the substrate outward toward the surface, as depicted in Figure 3(a).

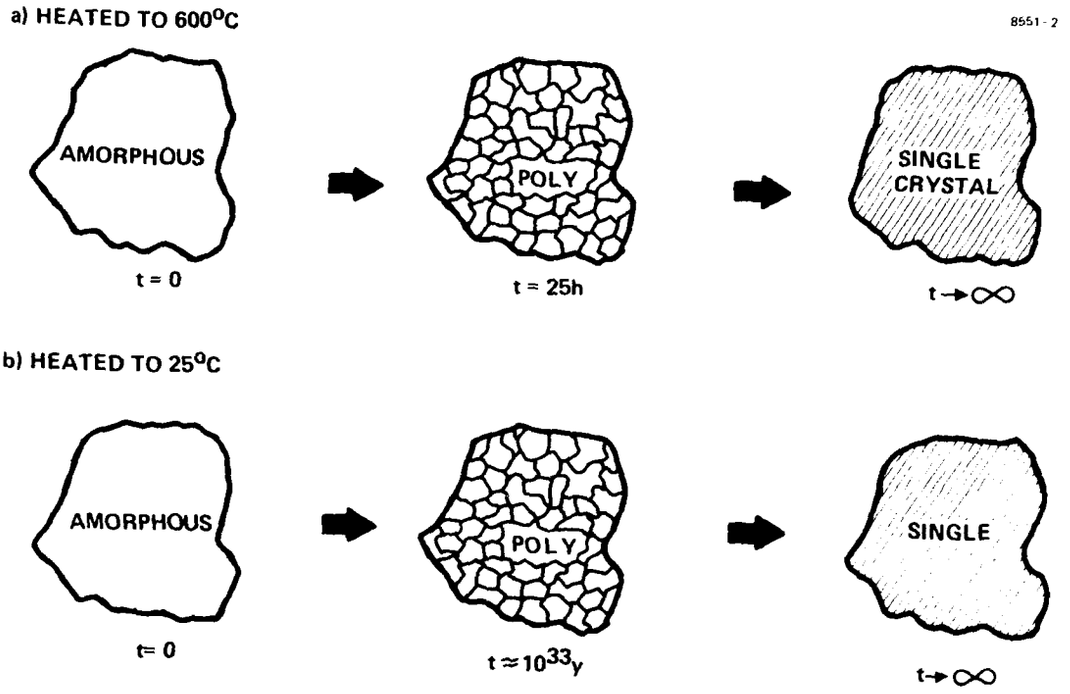


Figure 2. Crystallization of an imaginary "chunk" of amorphous Si heated in vacuum.

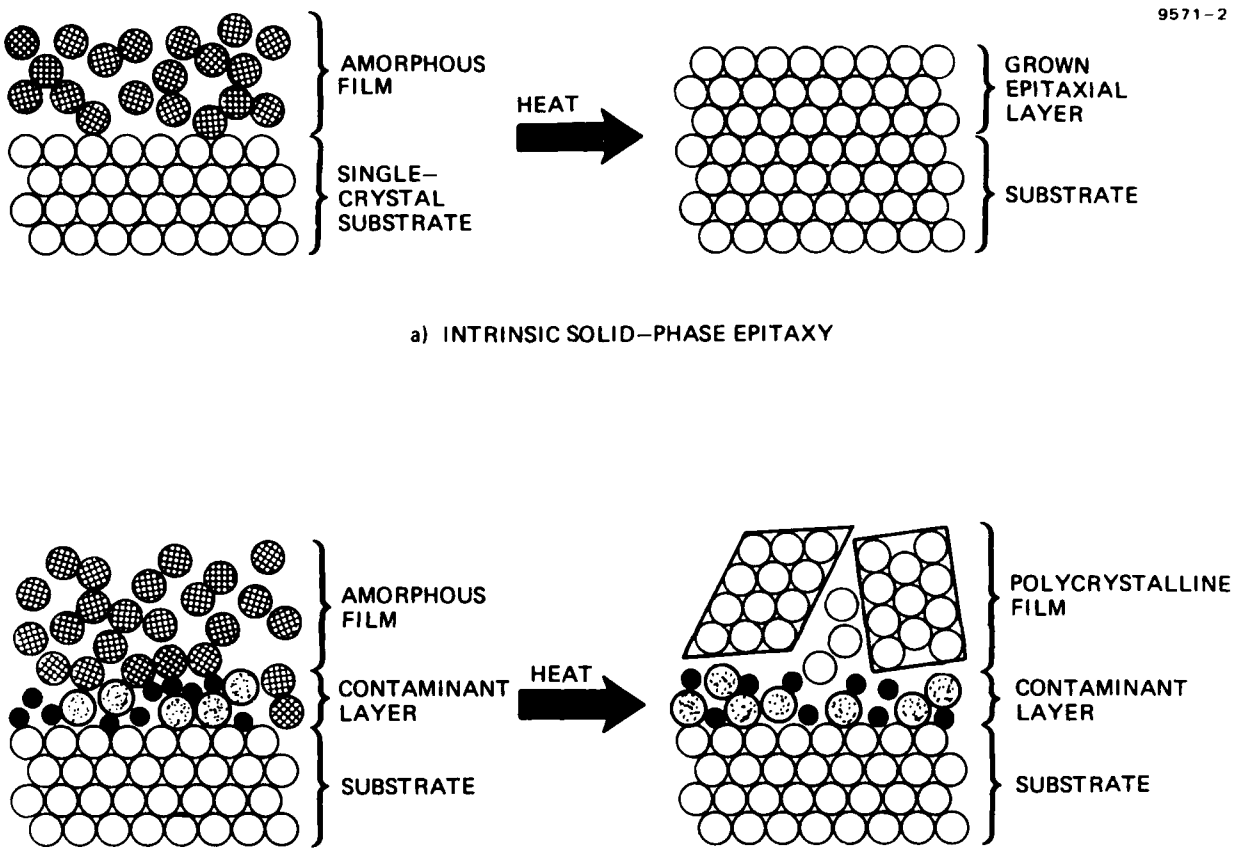


Figure 3. Crystallization behavior of deposited amorphous films: (a) ideal SPE in a totally contaminant-free sample; (b) random crystallite formation due to obscuration of the substrate by adsorbed contaminants.

In the absence of foreign impurities, the growth rate of SPE is usually rapid enough that the entire film will be converted into a single-crystal layer before any randomly oriented crystallites can form in the remaining unconverted portion of the amorphous film.

Impurities, however, can drastically modify the situation to the extent that SPE may not be able to occur at all. For example, if one attempts to perform SPE by depositing Si onto a single-crystal wafer, it is extremely difficult to achieve the intimate film/substrate contact required for epitaxy. In the case of Si, a native oxide forms very rapidly on the surface of the substrate during exposure of the crystal to any oxygen-containing ambient, leading to the situation depicted in Figure 3(b). The oxide and adsorbed foreign atoms prevent intimate contact between film and substrate. In this circumstance, only random crystallization can occur during heating. Thus, a prerequisite for achieving SPE in deposited films is the elimination or dispersion of substrate contaminants.

Contaminants can interfere with or inhibit SPE in other ways too. If the amorphous film contains foreign impurities, either because of poor vacuum during deposition or subsequent exposure to a contaminating ambient, then the kinetics of SPE can be altered to such an extent that other processes such as polycrystallization may become competitive. As shown in Section 4, the concentrations of foreign atoms necessary for significant disturbance of SPE are fairly low, and very careful processing must be used to avoid contamination.

Because of the high sensitivity of SPE to contaminants, intrinsic SPE of deposited films has only been achieved in a few materials. Prior to our work, Cho[1] used UHV processing to obtain SPE of thin (<300 Å) layers of GaAs on GaAs and GaP. The key to success in Cho's experiments was the ability to produce a clean substrate by thermal decomposition of the surface in UHV. This technique works well for III-V materials, but not for Si, where much higher temperatures are required. However, by using in situ inert gas sputter-etching followed by thermal annealing, Jona[2] was able to produce clean Si surfaces in UHV and observed the room-temperature crystallization of deposited films up to about 30 Å

in thickness. No attempt was made to convert thicker amorphous films to epitaxial layers by heating.

Attempts by other groups[3,4] to obtain SPE of Si deposited onto Si wafers were unsuccessful due to the lack of proper in situ substrate cleaning. However, a very intriguing process was developed at Caltech[5] for avoiding the substrate contaminant problem. They deposited a transition-metal film onto Si prior to deposition of the amorphous Si. Then, heating to 250°C was used to cause silicide formation. During the silicide reaction, the native oxide initially present on the substrate evidently was dispersed. Further heating to 450 to 560°C was observed to cause transport of Si through the silicide and epitaxial growth at the substrate/silicide interface. Unfortunately, films grown by this process contained a high (>0.1%) concentration of retained metal atoms, making them unusable for microelectronic applications. Moreover, the concentration of retained metal was found to depend inversely on impurity content in the deposited Si.[6,7]

The possibility of contaminant effects in the studies of silicide-interlayer SPE at Caltech made it difficult to determine the intrinsic behavior of the process. Consequently, we decided to study silicide-interlayer SPE in UHV, in the absence of gross contamination. Section 3 presents our findings on the metal-interlayer approach to SPE and shows that the process proceeds quite differently when conducted in contaminant-free conditions. Our principal conclusion is that contaminant effects dominated all the prior work on SPE. Furthermore, our results indicate that silicide-interlayer SPE is not suitable for microelectronic applications, even when performed in UHV.

We subsequently turned to studies of the intrinsic SPE of Si films deposited directly onto Si wafer substrates. By employing UHV techniques, we obtained good epitaxial quality in layers grown on Si(100), and made transistors in such films to test their suitability for device applications. Section 4 reports this work, including examples of the orientation dependence and thickness dependence as well as studies of methods of dopant introduction and dopant atom behavior during SPE growth.

The effects of contaminants on direct (Si/Si) SPE are also reported in Section 4. Contaminants present on the single-crystal substrate in sub-monolayer quantities are shown to cause a high defect density and extreme surface roughness in SPE. Even when the substrate is clean, exposure of a deposited amorphous Si film to room air is shown to result in deep penetration of both C and O. Thus, when intrinsic SPE is performed in a vacuum furnace after air exposure of the deposited film, a thin polycrystalline layer forms on the surface. To grow device-quality films by SPE, the entire process must be conducted in UHV.

Since the key element in our work on SPE was UHV processing, some of the equipment specially constructed for this purpose is described in Section 2. The critical processing steps for successful SPE are also detailed there. Section 5 summarizes our conclusions and offers suggestions for future work on SPE.

The experimental work reported here was conducted primarily by J.A. Roth, who had responsibility for the technical direction and implementation of the project goals. Technical assistance was provided by A.J. Mohr and R.F. Scholl. C.L. Anderson, head of the Solid-State Electronics Section in the Chemical Physics Department at HRL, initiated the Solid-Phase Epitaxy program and provided overall technical and administrative guidance throughout. Rutherford backscattering analysis (RBS) was performed skillfully and cheerfully by H.L. Dunlap. L.D. Hess and G.L. Olson conducted the laser annealing of SPE specimens. M. von Allmen of Caltech assisted in the formulation and interpretation of the laser-annealing experiments.

Throughout this work, we benefited greatly from technical discussions with our colleagues at Caltech, J.W. Mayer, S.S. Lau, M-A. Nicolet, and Z.L. Liau. We are particularly indebted to S.S. Lau for performing channeling analyses and to W.F. Tseng (now at NRL) for providing TEM micrographs that were instrumental in establishing the feasibility of direct SPE.

The continuing support and encouragement of Larry Cooper of ONR are gratefully acknowledged. His superb technical intuition and willingness to provide a research environment unfettered by over-administration were instrumental in the success of our program.

SECTION 2

EXPERIMENTAL APPARATUS AND MEASUREMENT TECHNIQUES

To determine the intrinsic properties of SPE, it was imperative to provide a noncontaminating ambient in which samples could be prepared and analyzed with minimal perturbation by foreign species. This requirement was met by performing most of the experimental work in UHV at pressures less than 10^{-7} Pa. To accomplish this, a commercial vacuum system, Ultek Model TNB-X, was equipped with a cylindrical mirror electron energy analyzer (CMA), for Auger spectroscopy, and a low-energy electron diffraction (LEED) unit of the four-grid display type, and modified to permit in situ thin-film deposition and several types of specimen treatments, such as heating and ion sputter etching. Since some of the facilities constructed for this purpose were crucial to the achievement of the experimental objectives and have more general applicability to other UHV surface and interface related experiments, they are described in detail below. Section 2.A describes the vacuum system and the functions and capabilities of the associated components used for in situ sputter cleaning, sample heating, and ion sputter etching. The specific techniques used for acquiring Auger electron spectra are detailed in Section 2.B, which also describes the methods used to obtain compositional depth profiles by combining ion-etching with Auger spectroscopy. Finally, Section 2.C presents the procedures used for preparing silicon substrates.

A. VACUUM SYSTEM AND COMPONENTS

1. Main Vacuum Chamber and Gas-Handling Subsystem

A schematic of the experimental vacuum chamber and its principal components is shown in Figure 4. The main system is composed of a 12-in.-diameter stainless-steel bell jar with all-metal seals, plus an auxiliary subsystem for gas handling and admission to or removal from the main chamber. The main chamber is pumped by a 200 liter/sec ion pump, which can be assisted by Ti getter pumping and/or cryopumping by

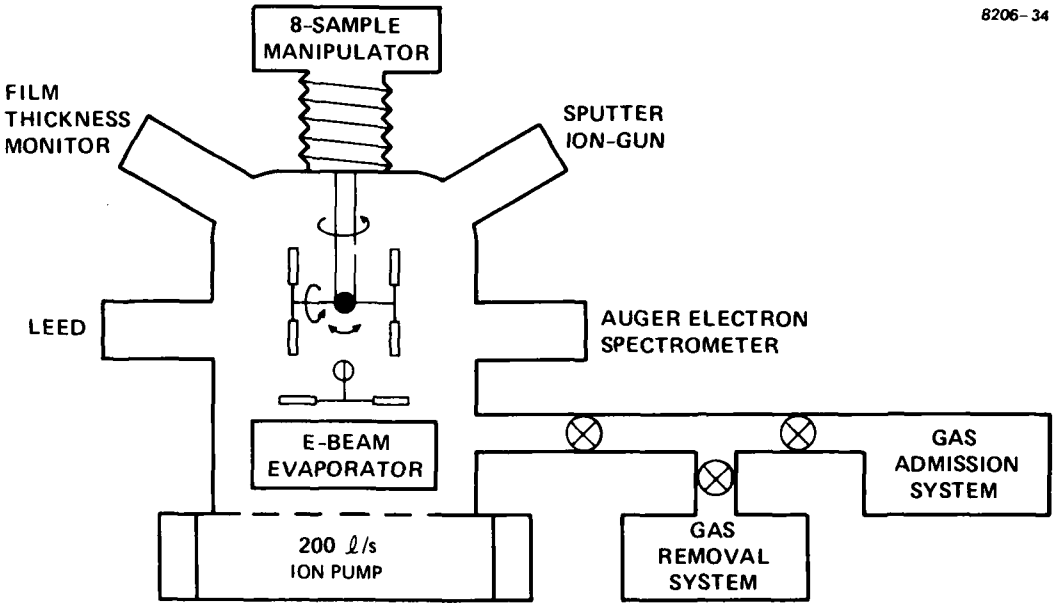


Figure 4. The experimental vacuum system and components.

an LN_2-cooled shroud which surrounds the Ti sublimation source. Rough pumping is done with sorption pumps filled with Linde 3A molecular sieve material and chilled by LN_2. The gas-handling subsystem, built especially for these experiments, consists of two components: (1) a pumping station and (2) a gas admission manifold. These actually constitute a second UHV system which interfaces with the main system through either a variable leak valve for controlled gas admission or a standard metal-sealed valve for gas removal from the main chamber.

Figure 5 shows schematically the components of the gas-handling subsystem and its connection to the main chamber. The entire system up to the valves on the gas cylinders can be baked to 200°C. Bakeout permits a vacuum of $<2 \times 10^{-7}$ Pa to be achieved and ensures minimal contamination of pure gas stored in the manifold. An important feature is the ultra-clean sorption pump labelled No. 1 in Figure 5. By first baking this pump into sorption pump No. 2 and then into the ion pumps, the molecular sieve material in the pump could be made clean enough to allow the pump to be used at pressures as low as 10^{-6} Pa. The primary application of this capability was in the removal of Ar from the main bell jar after sputter etching a specimen. The use of an auxiliary ion pump instead of the main ion pump to remove Ar after sputtering (1) substantially increases the usable life of the main ion pump elements and (2) virtually eliminates recontamination of a clean sample surface by contaminants regurgitated in the ion pump during start-up.

An important measure of the vacuum integrity of a surface analysis UHV system is the rate at which pressure rises in the absence of pumping. This quantity, dP/dt, can be used to estimate the flux of contaminant gas molecules onto a sample surface during ion-milling or sputter-etch cleaning, when the main pump is ordinarily off. Additionally, dP/dt gives the rate of contamination of gas stored in the gas manifold. Representative values for the main chamber and gas-handling systems used in this work are given in Table 1.

An example of the value of these excellent vacuum conditions is in the use of Auger spectroscopy to obtain a depth profile of the oxygen content in a thin film. Such a profile is obtained either by continuously

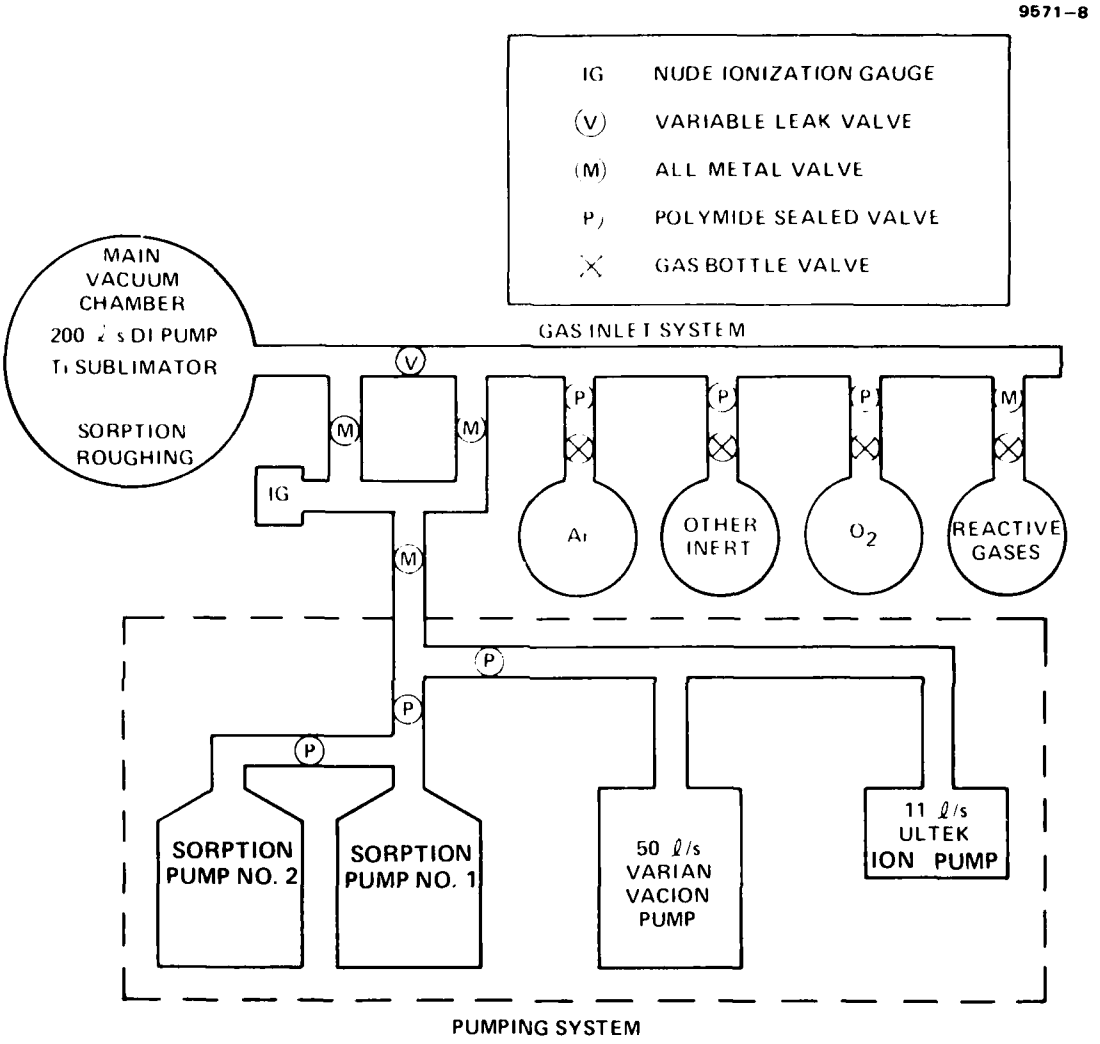


Figure 5. Subsystem for pure gas admission and removal.

Table 1. Vacuum System and Gas-Handling Subsystem Performance

	Base Pressure, Pa	dP/dt, Pa sec^{-1}	Ar Contamination Rate, ppm hr^{-1}
Main chamber	$<10^{-8}$	$\lesssim 5 \times 10^{-10}$(a)	360(c)
Gas-handling subsystem	$<10^{-6}$	$\lesssim 2 \times 10^{-7}$(b)	1.2(d)

[a] Ion pump off, cryoshroud chilled by LN_2, ion gun filament on.

[b] No pumping whatsoever.

[c] Ar pressure 5×10^{-3} Pa for sputtering

[d] Ar pressure ~800 Pa in holding manifold after transfer from gas bottle.

or by intermittently recording Auger spectra while ion-milling (sputter-etching) the film. In the case of continuous milling, a steady-state balance will be established between the rate of adsorption of oxygen from the ambient onto the sample surface and the rate of oxygen removal by sputtering. The resultant Auger signal of adsorbed oxygen can thus be erroneously interpreted as representing oxygen in the bulk of the specimen.

The steady-state surface coverage of oxygen due to contamination from the ambient during sputtering can be written as:

$$\theta \simeq 7.5 \times 10^{3} P_{ox} \cdot \eta \cdot R^{-1} \text{ monolayers},$$

where P_{ox} is the partial pressure (in Pa) of gases containing oxygen, η is their average sticking probability, and R is the sputter-etch rate in monolayers/sec. From the discussion above, we can expect P_{ox} to increase with time proportional to the total pressure rise rate dP/dt. Using $dP_{ox} = dP$ as a worst-case estimate and assuming unity sticking probability for oxygen, we can write:

$$\theta = 7.5 \times 10^{3} \ (dP/dt) \cdot T/R^{2} = 3.75 \times 10^{-6} \ T/R^{2} \text{ monolayers},$$

where T is now the total film thickness milled off (i.e., the depth of analysis, in monolayers). Thus, the effect of imperfect vacuum is to create a spurious oxygen signal which increases with depth. A slightly different way of expressing this result is to specify the maximum film thickness that can be profiled before adsorbed oxygen begins to produce an observable Auger signal. In actual operation, it was possible to profile Si films as thick as 5000 Å with no evidence of oxygen adsorption.

2. Non-Contacting UHV Specimen Heater

Many instances arise where it is necessary to heat a thin (wafer) specimen in the UHV chamber. In the present experiments, the requirement to anneal lattice damage caused by inert gas sputter-etching, as well as the need for heating to cause thin film reactions, necessitated the development of a technique for heating samples to temperatures as high as 1000°C, without producing either contamination or physical distortion of the wafer. Uniformity of temperature across the sample surface was also a consideration, the goal being ±10°C over a 1/2 in. square sample.

Several different methods can be used to heat samples in UHV, but most have shortcomings when extended to the temperatures required to anneal sputter damage in Si ($\gtrsim$850°C). The basic problem is the difficulty of obtaining reliable thermal contact between a Si wafer and a solid hot

object in UHV without stressing the wafer. Stress is undesirable since at elevated temperatures it is relieved by the generation of dislocation (slip) networks. Thus, non-contact heating is highly desirable. Techniques used in the past include: Joule heating (I^2R heating caused by passing a current through the wafer), radiant heating by light from an external bright lamp focused on the sample surface, and direct electron bombardment. Joule heating requires electrical contact to the wafer, and, moreover, the sample must be specially shaped to achieve uniform heating. Use of an external lamp requires a high-brightness source and cumbersome optics to heat Si to >850°C. Direct electron bombardment suffers from gross temperature non-uniformities unless a sophisticated electron optics beam-scanning system is used. Thus, these techniques were deemed inadequate for the present experiments, and a simpler, more effective method was developed.

A high-temperature noncontact heater was created by electron bombarding a thin tungsten or tantalum disc and allowing radiant energy from the disc to heat a sample placed close to it. A very simple hot filament electron gun (*Physical Electronics Industries Model* 04-121) was modified to permit the support of a 25-mm- or 55-mm-diameter W disc approximately 5 cm beyond the end of the gun filament. The disc is supported by four W wires, each balled on its end by melting, which just protrude through holes near the perimeter of the disc. The modified gun mounts on a standard 2-3/4-in. metal-sealed UHV flange.

In operation, a Si specimen, mounted on its Ta holder, is placed ∿1.5 mm from the W disc. During heating, the disc is viewed from the opposite (gun filament) side with a pyrometer to determine its temperature. Direct measurement of wafer temperature was attempted without success. Therefore, a series of calibration experiments was performed to relate the temperature of the W disc to that of the Ta mounting pad. Then, the equations expressing radiative transfer of energy between the disc, Si wafer, and Ta mounting pad were solved to obtain a relationship between T_{disc} and T_{sample}. The calculated dependence is approximately

$T_{sample}^{(°C)} \simeq 0.6\ T_{disc}$ for temperatures near 800°C. Thermal conductivity of the disc and multiple bounces of radiation between disc and sample average out nonuniformities of the incident electron beam and result in less than a 10°C spread across a 12 mm wafer. Additionally, the inertness of W ensures that the sample is not contaminated during heating. For improved temperature control in long-term annealing, a feedback circuit which used the pyrometer output was added to control the heater power supply.

3. Electron-Beam Evaporator

A 3-hearth electron-gun evaporator (Thermionics, Inc. Model 100-0030) was installed in the UHV chamber to permit depositing films of transition metals or Si for the present experiments. All substances were evaporated directly from the Ni-plated Cu hearths without liners in order to minimize contamination in the films. With the substrate placed 15 cm from the source, deposition rates of up to 2 Å/sec could be achieved for Pt and Nb, up to 30 Å/sec for Pd, and up to about 5 Å/sec for Si, although most depositions were performed at lower rates than these. After extensive operation of the source for degassing, excellent pressures could be maintained during film deposition. A measure of the film purity achieved is given by the observation that even for Nb, which strongly getters oxygen, films could be produced that had less than 500 ppm oxygen.

Thicknesses of the deposited films were inferred from the indications of a quartz crystal oscillator placed $\sim$70 cm from the evaporation source. This monitor was calibrated against thickness measurements made by Rutherford backscattering, surface profilometry (Dektak), and optical interferometry. By comparing measurements made over a span of several months, we determined that the quartz crystal indications were accurate to within ±10%, which was sufficient for the intended experiments.

B. SAMPLE PREPARATION AND DIAGNOSTIC PROCEDURES

1. Silicon Substrate Preparation and Mounting

Substrates for SPE were prepared from commercially available, polished 5-cm—diameter Si wafers with either <001> or <111> surface orientation. In most experiments, the wafers were diced into 12.7 mn squares either by scribing and breaking or by sawing with a diamond-impregnated cutting wheel. In either case, it was found that the dicing operation generated a fine dust of Si particles which attached themselves tenaciously to the polished surface. No chemical treatment short of repolishing was found to remove the particles, and thus a means had to be developed to passivate the wafer surface during dicing. The complete process developed for this purpose is shown in Table 2.

For manipulating samples in the UHV chamber, each square of Si was mounted loosely on a specially designed Ta pad which incorporated retainers to keep the wafer from falling off without stressing the wafer. The mounting technique is illustrated in Figure 6. Up to eight samples could be handled by a multi-function manipulator and sample support mechanism designed to give each sample access to any of the processing and diagnostic facilities in the UHV chamber.

2. Silicon Cleaning in UHV

For experiments utilizing bare Si substrates, a procedure was developed for producing extremely clean and crystalline surfaces as evidenced by AES and LEED characterization. Except for a few instances where it was desirable to study interactions or contaminated surfaces, this UHV cleaning treatment was used for all SPE samples.

Two basically different approaches exist for removing the surface contaminants from Si in preparation for surface sensitive experiments: (1) heating to achieve thermal decomposition of the surface oxide, and (2) inert gas ion sputter-etching followed by heating to anneal the sputter-induced damage and release embedded atoms of Ar. The former

Table 2. Procedure Used to Produce Si Substrates for UHV SPE

1	Initial contaminant removal	a. Ultrasonic: TCE, ME, DIW b. Etch in 4:1:1 H_2O:H_2O_2:NH_4OH, 10 min, 80°C; DIW rinse c. Etch in 49% HF d. Etch in 4:1:1 HCl:H_2O:H_2O_2, 10 min, 80°C; DIW e. Blow dry, filtered N_2
2	Oxidize	Wet O_2, 1050°C, ~1500 Å SiO_2
3	Photoresist overcoat	a. Spin 2000 rpm, 30 sec, preferred side b. Paint on backside c. Normal pre-bake
4	Mount for sawing	Wax onto dummy Si wafer with paraffin
5	Saw	Saw clear through
6	Wax/resist removal	a. Spin-off resist at high speed b. Recoat and spin again c. Loosen dice in TCE d. Ultrasonic in TCE (remove wax) e. Ultrasonic in acetone (remove resist) f. Rinse in TCE, acetone, DIW
7	Si dust removal	Stir etch in 10:3:0.5 HNO_3:CH_3COOH:HF (etches Si 50X faster than SiO_2)
8	SiO_2 removal	a. Etch SiO_2 in BOE b. Rinse DIW
9	Final contaminant removal	a. Same as Steps 1.a through 1.c b. Blow dry, filtered N_2

TCE = trichloroethylene
ME = methanol
DIW = >17 MΩ deionized water
BOE = Allied Chemical BOE™ 930 buffered oxide tech

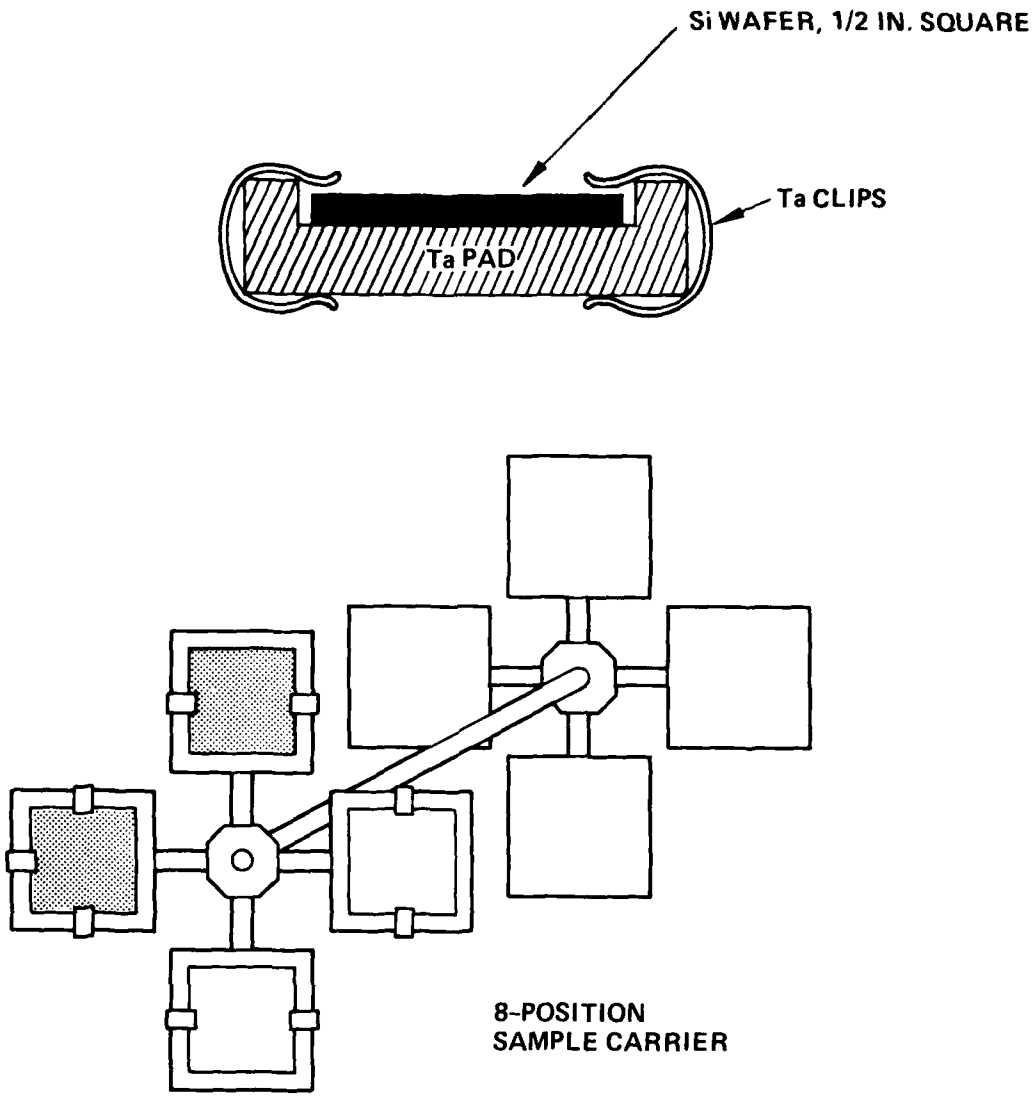


Figure 6. Stress-free mount for manipulation of up to 8 samples in the UHV chamber.

treatment is only successful if hydrocarbon contaminants are strictly localized on the outer oxide surface. Then they are evidently desorbed along with the decomposing oxide. However, carbon distributed within the oxide, at the silicon/oxide interface, or even near the Si in the case of a thin, non-uniform oxide, has a high probability of bonding to the Si during heating to form Si-C particles or clusters[8]. Once formed, these can only be removed by heating to over 1200°C, a procedure which usually leaves the Si surface covered by a high density of thermal etch pits which give it a "frosted" appearance.

A more reliable procedure is a sputter/anneal treatment which we have used exclusively. Approximately 50 Å of material, mostly oxide and contaminants, is ion etched from the surface using 2-keV Ar^+ at near-normal incidence. Alignment of the ion beam along the surface normal is avoided to minimize deep channeled implantation of the inert gas ions. After sputtering, the wafer is heated to 850 to 950°C to release implanted Ar and restore the surface crystallinity. After this treatment, AES finds no surface contaminants (to less than 0.001 monolayer) and LEED measurements indicate that the appropriately reconstructed equilibrium surface has been attained (Si<100>:2 x 1 or Si<111>:7 x 7). The Si<111> surface seems less tolerant of excessive anneal temperatures, and thermal etching has occasionally been observed on these surfaces when the temperature was accidentally allowed to exceed ~1050°C.

Once prepared in a clean condition, Si surfaces could be maintained for several days in the UHV system with only minor (0.001 monolayer) accumulation of adsorbates (usually O and C). One concern for thin-film sequential deposition experiments is the extent to which a clean Si surface may become re-contaminated during run-up of the E-gun evaporator or during deposition on another part of the wafer through a mask. We examined this directly and found that no measurable O or C adsorption occurs during run-up if the evaporator has previously been thoroughly outgassed.

3. Auger Electron Spectroscopy

Electron-excited Auger spectra were obtained by bombarding samples with 3-keV electrons and measuring the kinetic energy distribution of the emitted electron current. Electron kinetic energy distributions were measured with a commercially available electrostatic velocity analyzer of the single-pass cylindrical mirror type (Physical Electronics Industries Model 21-118-G).

High-resolution depth profiles were produced by combining AES with in situ ion sputter-etching. As deeper portions of the sample were exposed by etching, the composition within the outer 10 to 20 Å at each depth was sampled via the Auger spectrum. By repetitively applying the sputter-etch/Auger spectrum sequence, plots were generated of the various Auger currents from different elements as a function of depth in the specimen. Sputter-etching was performed in a manner such that the area of the sample within which Auger electrons were produced was sputtered at a uniform rate. This was ensured by rastering the sputter ion beam over an area larger than the Auger primary electron beam at its focal point on the sample surface.

Typically, ion sputtering was performed by turning off the main vacuum pump and then admitting research-grade Ar gas to a pressure of 6.5×10^{-3} Pa. During sputtering, a copper shroud located in the ion pumping well was kept cold by contact with an internal liquid nitrogen reservoir filled from a LN_2 dewar. This mild cryopumping aided in holding down the gradually rising partial pressure of condensable gases desorbed continuously from the vacuum chamber walls. An ion current of $\sim$20 $\mu A/cm^2$ was used for depth profiling.

SECTION 3

SILICIDE-INTERLAYER SPE

As discussed in Section 1, direct SPE of a deposited film on Si would ordinarily be prevented by the presence of a native oxide on the substrate surface prior to deposition of the amorphous film. However, early workers in SPE found that a metal film deposited onto the Si substrate was partially effective in dispersing the native oxide and producing a suitable environment for nucleation and growth of Si transported through the metal. Some of the earliest work used simple metals such as Al[9], Ag[10] and Au[11] deposited onto the substrate before deposition of amorphous Si. The metal was thought to function as a travelling solvent that supplied Si atoms dissolved from the amorphous Si overlayer to the substrate/metal interface. However, with simple metals, the nucleation and growth of Si was often sporadic and nonuniform, suggesting that the reaction between Si and non-transition metals is not vigorous enough to break up the native oxide uniformly.

Canali et al.[5,12] used a transition metal such as Pd for the interlayer, instead of a simple metal as had been used earlier. Subsequent heating caused formation of a transition-metal silicide through the solid-state reaction of metal with Si from the single-crystal substrate on one side and the amorphous film on the other. In the case of Pd_2Si, the silicide reaction apparently has the effect of dispersing the substrate oxide and contaminants, providing a "virgin" interface for subsequent epitaxial growth.

The silicide-interlayer approach to SPE as employed by Canali and others at Caltech is illustrated in Figure 7. First, Pd is deposited to form a Si(crystal)/Pd/Si(amorphous) sandwich, as in Figure 7(a). Initial heating of this Si(C)/Pd/Si(a) structure causes formation of Pd_2Si, shown in Figure 7(b). Presumably the oxide and hydrocarbon contaminants become dissolved in the silicide. Further heating to temperatures in the range 500 to 600°C then causes Si from the amorphous

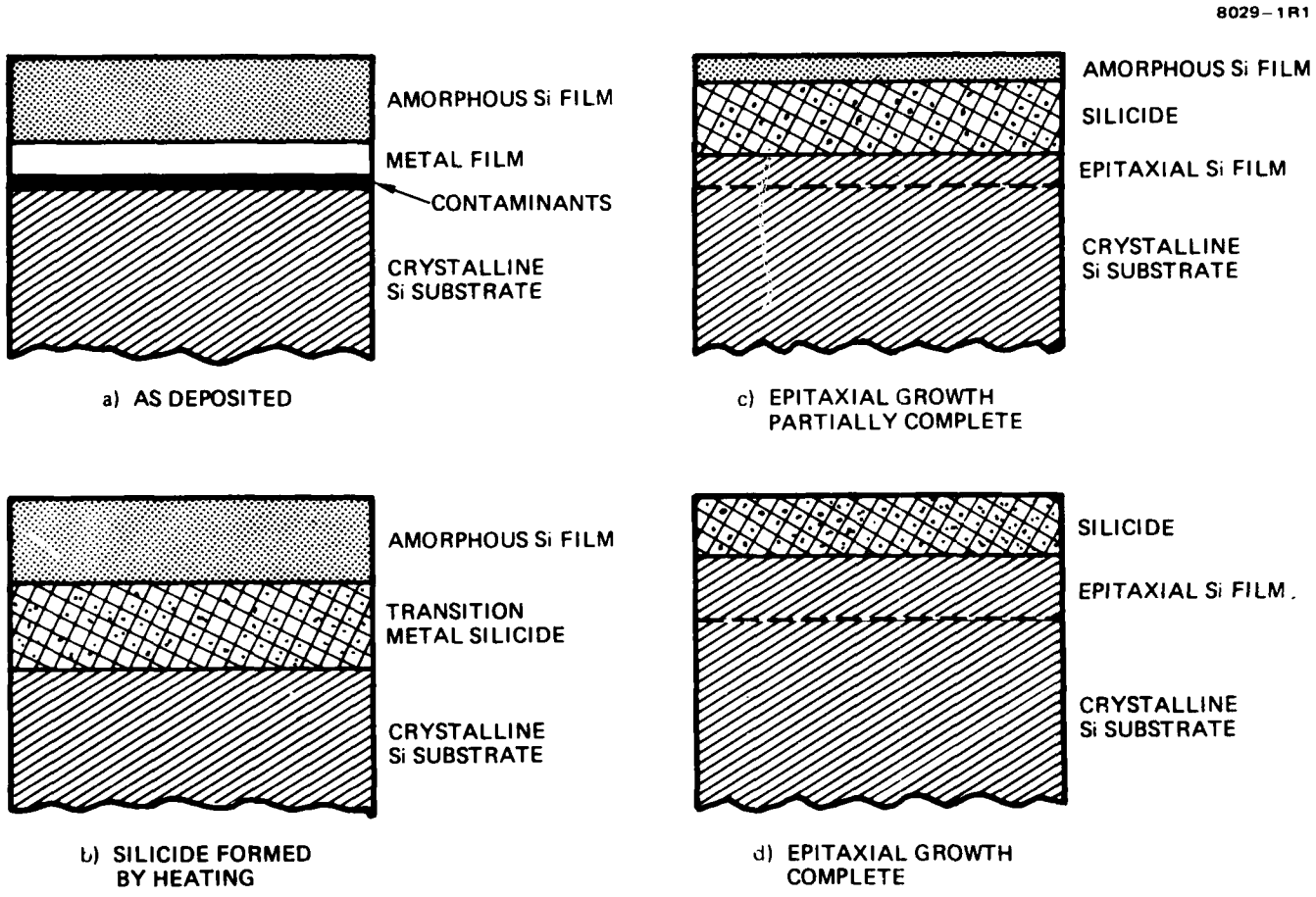


Figure 7. Silicide interlayer approach to SPE.

layer to appear at the Si(c)/Pd_2Si interface where it crystallizes epitaxially (Figure 7(c)). The final outcome of silicide-interlayer SPE is shown in Figure 7(d). In the Caltech experiments, Pd_2Si was found to be uniformly displaced to the outer surface, and all of the original Si(a) film was incorporated into an epitaxial layer beneath the silicide.

During a systematic study of interlayer SPE growth rates, Liau[6,7] found that carbon inadvertently incorporated in the amorphous Si films deposited at Caltech played a critical role not only in determining the growth rates but also in affecting the quantity of Pd trapped in the resulting epitaxial Si layer. In the absence of measurable carbon, Pd trapping was very large, but with about 1% C, films having less than 0.1% trapped Pd could be grown. In examining the substrate preparation techniques and film deposition conditions used in the Caltech work, it became apparent to us that other contaminants besides carbon might also be important in determining the outcome of silicide-interlayer SPE, so we proposed to reproduce the Caltech process in a noncontaminating ambient. Our goal was to establish which features of silicide-interlayer SPE (e.g., Pd trapping) were intrinsic and which were contaminant-related.

Our approach was to perform SPE in a UHV system equipped with substrate preparation, film deposition and in situ analytical capabilities. In this manner, we eliminated or at least minimized several potential sources of contaminant introduction that had existed in the earlier work. Substrate contaminants were removed in UHV by argon ion sputter etching. Film depositions were performed at pressures below 10^{-6} Pa, ensuring good purity of the initial layers. E-beam deposition without hearth liners eliminated carbon contamination in the deposited amorphous Si. All heating for silicide formation and subsequent epitaxial growth could be conducted in the UHV chamber at pressures below 4×10^{-7} Pa. In an attempt to delineate the sources of contaminants and their effects, we also performed experiments in which samples were partially processed in

UHV then removed to an independent vacuum furnace capable of $<2 \times 10^{-4}$ Pa operation during heating.

Our main result was that silicide-interlayer SPE does not intrinsically (i.e., in the absence of contaminants) behave as depicted in Figure 7. By comparing samples processed entirely in UHV with equivalent samples processed partially outside of UHV, we established that certain contaminants must be present for silicide-interlayer SPE to produce uniform growth and complete transport of silicide to the surface. Contrary to the Caltech findings[13], no difference in growth morphology was observed between <100>- and <111>-oriented substrates.

A. SPE WITH A Pd_2Si INTERLAYER

For the study of Pd_2Si-interlayer SPE, samples were prepared according to the four different processing schedules indicated in Table 3. We begin with a discussion of our findings on nominally uncontaminated specimens that were processed entirely within the UHV chamber.

Samples processed entirely in UHV gave the most significant result: in clean specimens, the silicide is penetrated by the growing epitaxial Si and suffers lateral fragmentation during growth. This produces a surface which consists of a mixture of epitaxial Si regions and Pd_2Si regions, rather than the uniform Pd_2Si surface that the Caltech workers found in contaminated specimens. The experimental data supporting this conclusion are now reviewed.

In-depth composition profiles showing the outcome of interlayer SPE conducted in non-contaminating conditions were obtained by a combination of AES and ion sputter etching. Typical results for a <111>Si substrate are presented in Figure 8. To arrive at the atom fractions of Si and Pd shown in the figure, the raw first-derivative Auger peaks were individually normalized to the signals from pure standards of freshly deposited Pd and Si films. The conversion of sputter time to depth into the specimen was based on independent Rutherford-backscattering analysis of the sample.

Table 3. Four Different Processing Sequences Used in Studies of Silicide-Interlayer SPE

1.	Pd deposited; Pd_2Si formed; Si(a) deposited; annealed in UHV.
2.	Pd deposited; Pd_2Si formed; Si(a) deposited; removed from UHV, annealed in vacuum furnace.
3.	Pd deposited; Si(a) deposited; Pd_2Si formed; annealed in UHV
4.	Pd deposited; Si(a) deposited; Pd_2Si formed; removed from UHV, annealed in vacuum furnace.

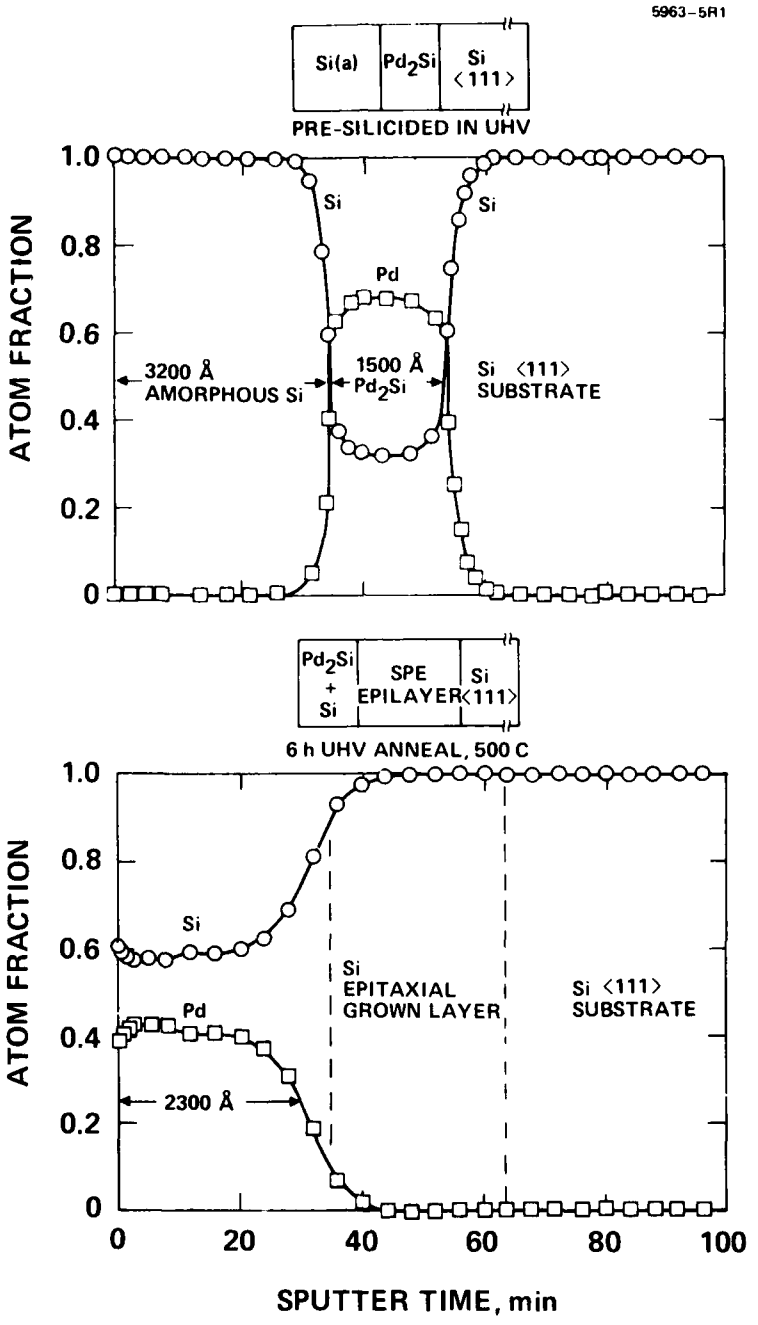


Figure 8. Auger sputter profiles of UHV SPE growth on Si(111) using a Pd_2Si layer.

Comparing the upper and lower panels of Figure 8 shows that annealing causes an interchange of Pd_2Si and amorphous Si layers, indicating that SPE occurred. But, after SPE growth, the region containing Pd_2Si is about 50% thicker than the original silicide layer, and the Pd atom fraction is only 43%, instead of the 67% expected for pure Pd_2Si. One possible interpretation of this result is that the outermost layer is not laterally homogeneous but consists instead of regions of Pd_2Si interspersed with regions of Si. This has been confirmed by a combination of SEM, RBS, and LEED analyses.

Figure 9 presents SEM micrographs of an SPE sample processed entirely in UHV. Figure 9(a) shows the surface of an Si <100> SPE sample that had been heated for 8 hr at 525°C in UHV. The white areas in the upper photograph were shown by energy-dispersive X-ray imaging to contain Pd and Si; dark areas are pure Si. Thus, the light areas are Pd_2Si.

The micrograph in Figure 9(b) was taken after the sample had been etched briefly in aqua regia to remove the Pd_2Si. The large pits left by the etching show that the Pd_2Si was totally interspersed with the Si in this sample after SPE growth. This explains the low Pd fraction indicated earlier by Auger profiling: since the area analyzed with our Auger instrument was at least 2500 times that shown in the SEM micrographs, the deduced Pd fraction was actually a lateral average over both Pd_2Si and Si regions.

To find out how deeply Pd_2Si penetrates beneath the surface of UHV SPE samples, 2 MeV RBS analysis was performed. In Figure 10 we present an RBS spectrum of the sample examined by SEM. For comparison, we have included a solid line showing how the spectrum would have looked if the Pd_2Si layer (originally 1350 Å thick, beneath 3700 Å of amorphous Si) had been uniformly displaced to the surface during growth. By carefully considering the relationship between energy loss and depth for Si and Pd_2Si, we showed that the Pd_2Si regions extend to ∿3160 Å below the surface. This indicates that only about 1500 Å of Si epi was grown

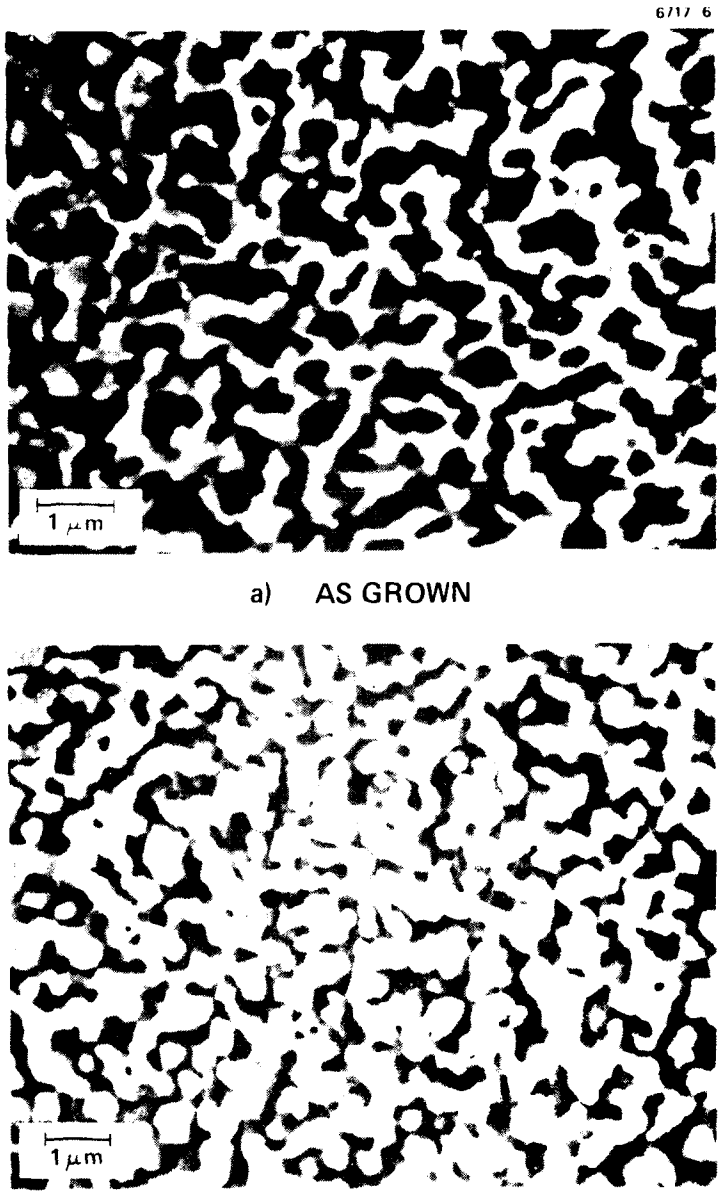


Figure 9.
Scanning electron micrographs of the surface of a UHV-processed Pd_2Si-interlayer SPE sample after growth.

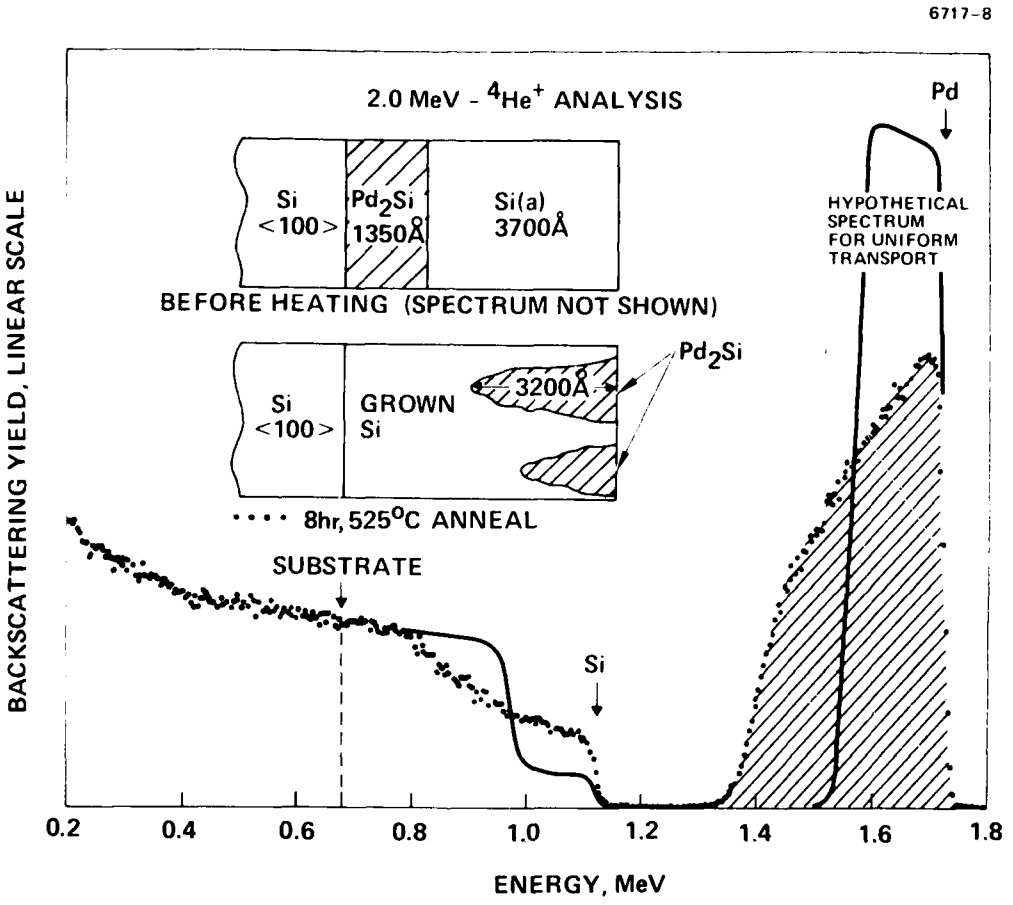


Figure 10. Rutherford backscattering spectrum of a Pd_2Si-interlayer SPE sample grown in UHV.

before the silicide broke up. This initial epi was shown by AES depth profiling to be free of Pd to less than about 0.05 at .%.

Examination of other samples having different silicide thicknesses has shown that SPE carried out under clean conditions only produces a Pd-free epitaxial layer slightly thicker than the original Pd_2Si layer. This finding is common to all UHV-processed samples so far examined, whether <100> or <111> oriented. Beyond the Pd-free region, the sample consists of spires or columns of Si leading to the surface, surrounded by Pd_2Si. Examination with RBS channeling-effect and LEED measurements of this outer region showed that the Si is everywhere epitaxial in spite of the complicated topography.

LEED analysis performed in situ also gave evidence that the Si in noncontaminated silicide-interlayer SPE samples is epitaxial. Pd_2Si on Si(100) does not exhibit a LEED pattern of its own. However, a well-contrasted LEED pattern characteristic of single-crystal Si(100) is seen on the surface of SPE samples. This pattern is in perfect registry with the LEED pattern from the Si substrate. Since LEED is sensitive to only the outer 1 or 2 atomic layers of a specimen, the observed pattern can only arise if the surface Si is part of an epitaxial layer extending all the way down to the substrate. The existence of epitaxial columns in clean Pd_2Si-interlayer SPE is also indicated by the RBS channeling-effect spectra shown in Figure 11. The sample used to obtain these spectra is not the same one shown in the earlier figures, but is similar in all respects. The channeling spectra show clearly that the Pd_2Si is not epitaxial (no difference between random and aligned spectra in the Pd region), but a distinct reduction in yield is observed from the Si (at energies below 1.1 MeV). The height of the Pd backscattering signal at the surface in comparison with that of Si shows that the surface contains only about 55% Pd instead of 67% for pure Pd_2Si. This implies a laterally mixed surface 82% of which is Pd_2Si and 18% crystal Si. Thus, out of all the Si present in the surface region, only 40% is crystalline. Therefore, the dechanneling caused by the non-epitaxial Pd_2Si accounts for a yield

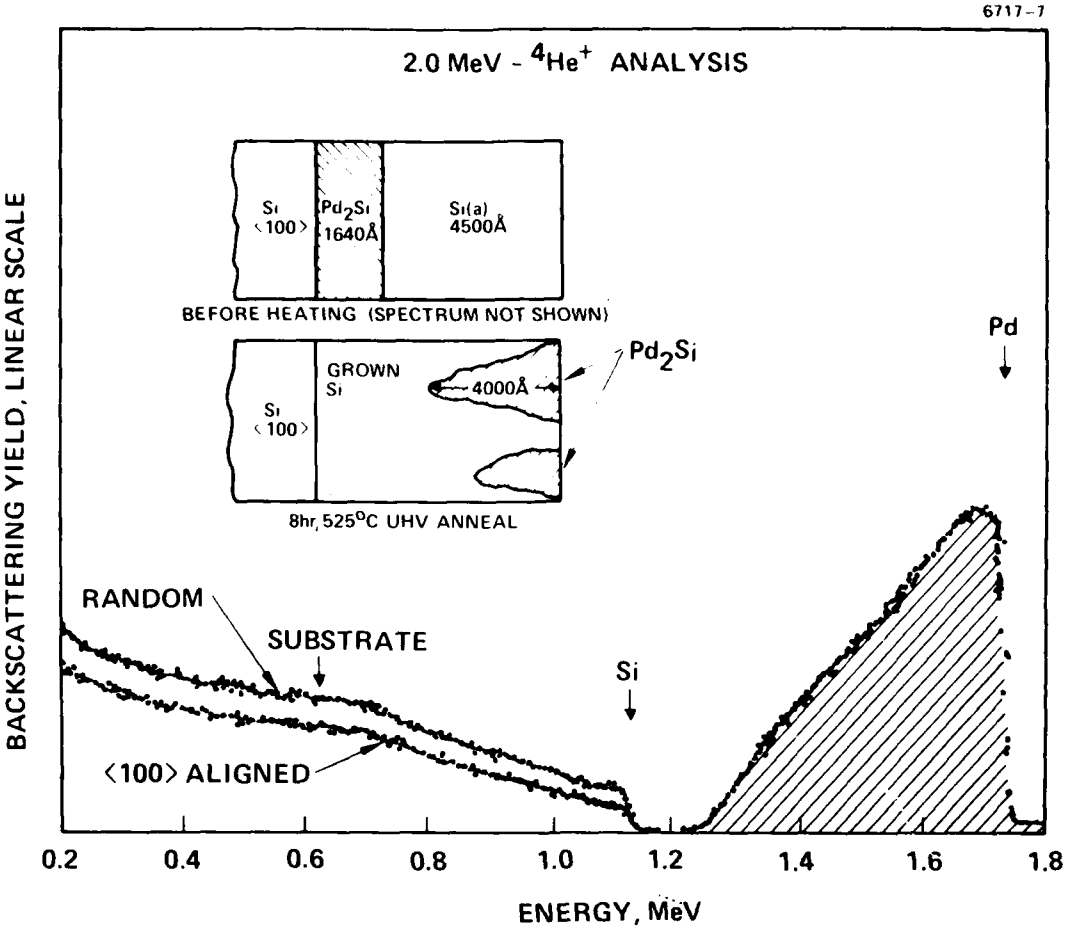
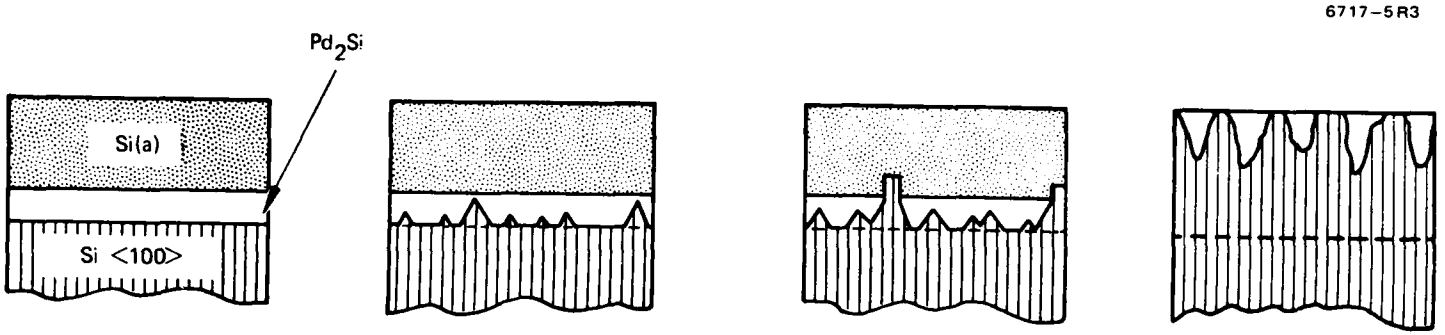


Figure 11. Channeling-effect spectra from an uncontaminated SPE sample grown in UHV for 8 hr at 525°C.

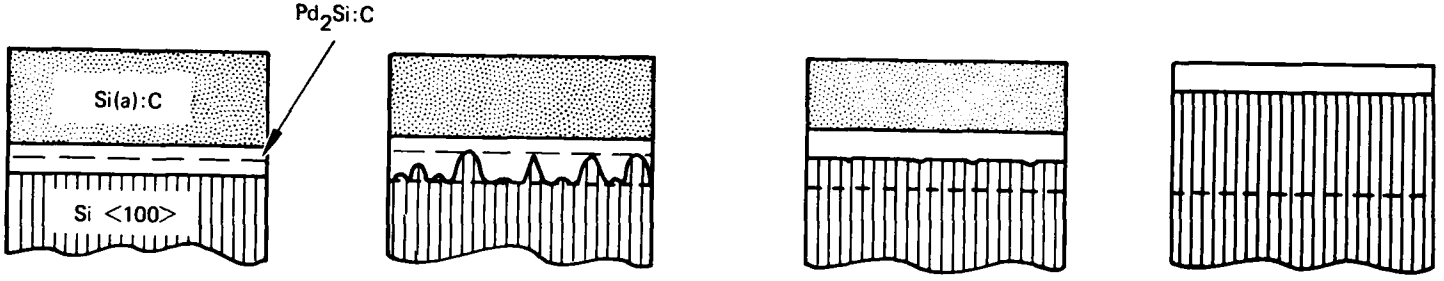
which is 60% of the random yield observed on the layer. Since the observed channeled yield near the surface is about 64% of the random yield, the remaining 4% dechanneling is the contribution from the epitaxial Si. This is a very respectable figure, and it shows that, within experimental error, the Si has good epitaxial crystallinity all the way to the surface, as had been suggested by LEED analysis.

The results presented in Section 4 demonstrate that the tendency of amorphous Si to form a single-crystal layer is very strong when contaminants are absent. This raises the possibility that Pd_2Si might actually obstruct the crystallization process in contaminant-free specimens. That is to say, given clean enough conditions, amorphous Si will grow epitaxially on a single-crystal substrate. Thus, for samples having a Pd_2Si interlayer, once a gap has been opened in the silicide, crystallization may proceed quite rapidly, forming columnar regions that reach to the surface. Quite possibly, the initial stage of growth prior to silicide breakup consists of nucleation and island formation similar to the "first transient" growth stage envisioned by Liau.[14] However, the Pd_2Si layer apparently develops "holes" at some time during heating, permitting the growth out to the surface that we have observed. The growth of columnar "grains" through openings in the Pd_2Si may occur simultaneously with a dissociative growth mechanism[15] that operates in regions still covered by Pd_2Si. In fact, some mechanism of this type must occur to account for the displacement of the Pd_2Si to the surface. Otherwise, the lateral development of the columnar grains would be expected to totally trap the silicide below the surface (which is contrary to the experimental findings).

A model for silicide-interlayer SPE based on our AES, RBS, and SEM/EDX analyses is presented in Figure 12, where it is compared to Liau's findings on carbon-contaminated specimens. We believe that penetration of the silicide is an intrinsic feature of Pd_2Si-interlayer SPE since the



a) INTERLAYER SPE, UNCONTAMINATED SAMPLE



b) INTERLAYER SPE, CARBON-CONTAMINATED SAMPLE

Figure 12. Comparison of models for Pd_2Si-interlayer SPE in uncontaminated and carbon-contaminated samples.

samples studied in our work are the least-contaminated specimens prepared to date. This hypothesis is further supported by the observation that pre-silicided and not-pre-silicided samples behave similarly provided all processing is done in UHV. Likewise, both <100>- and <111>-oriented substrates are found to behave identically in clean samples, whereas they act quite differently in the contaminated case.[13] These findings on a variety of clean specimens suggests that the behavior is intrinsic and that prior work was dominated by contaminant-induced effects.

In an attempt to partially simulate the annealing conditions employed in the work at Caltech, uncontaminated samples of Si<100>/Pd/Si(a) and Si<100>/Pd_2Si/Si(a) were prepared in UHV and then removed to a vacuum furnace for heating. In the case of the non-silicided samples, a preliminary anneal was used to first convert Pd into Pd_2Si prior to the epitaxy. A significant difference was observed in the outcome of SPE for samples prepared by these two different process schedules. Samples of Si<100>/Pd/Si(a) that were subjected to the two-step furnace anneal exhibited only partial epitaxy and were found to contain a very large buried distribution of Pd as well as a second Pd concentration peak at the surface. This conclusion is drawn from the RBS spectra in Figures 13 and 14 and is illustrated schematically in Figure 15. The RBS spectra show that a large fraction of Pd_2Si remains near the original Pd_2Si/Si(a) interface instead of being displaced to the outer surface during annealing. The existence of this additional "buried" silicide is unique to non-pre-silicided specimens annealed after air exposure. Their in situ-annealed counterparts do not exhibit a secondary, buried Pd peak (cf. Figure 10). We were led, therefore, to examine the possibility of contaminant introduction during the post-UHV processing to explain the observed trapping of silicide near the initial Pd_2Si/Si(a) interface.

Additional experiments on samples processed slightly differently showed that exposure to room air and/or furnace annealing cannot be solely responsible for silicide trapping. When the silicide reaction

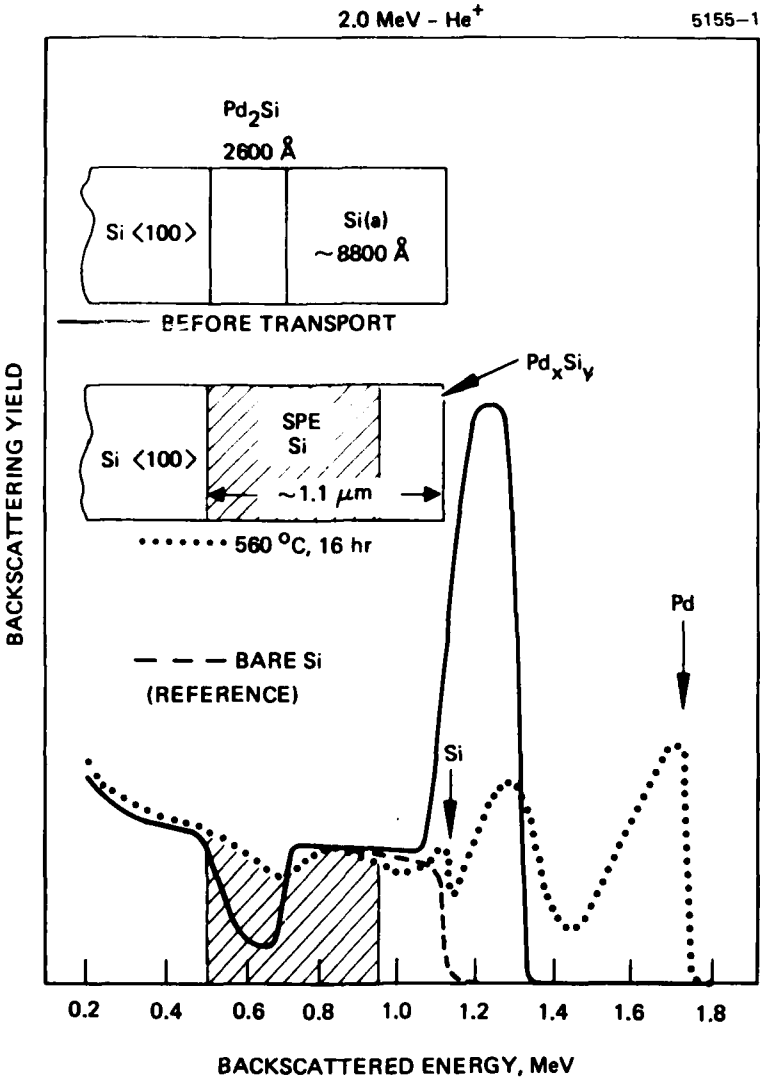


Figure 13. RBS spectrum of a Pd_2Si-interlayer SPE sample deposited in UHV then removed to a vacuum furnace for silicide reaction and epitaxial growth.

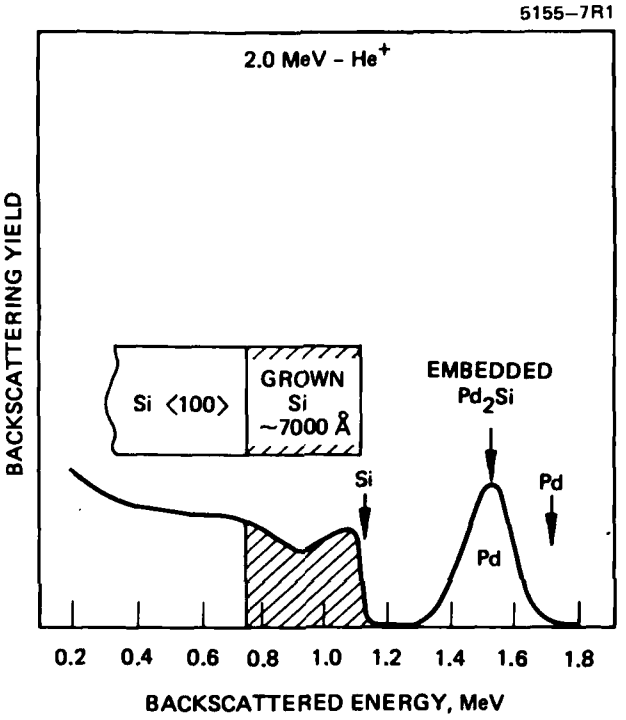


Figure 14.
RBS spectrum from same specimen as in Figure 13 after removal of outer 4500 Å by sputter etching.

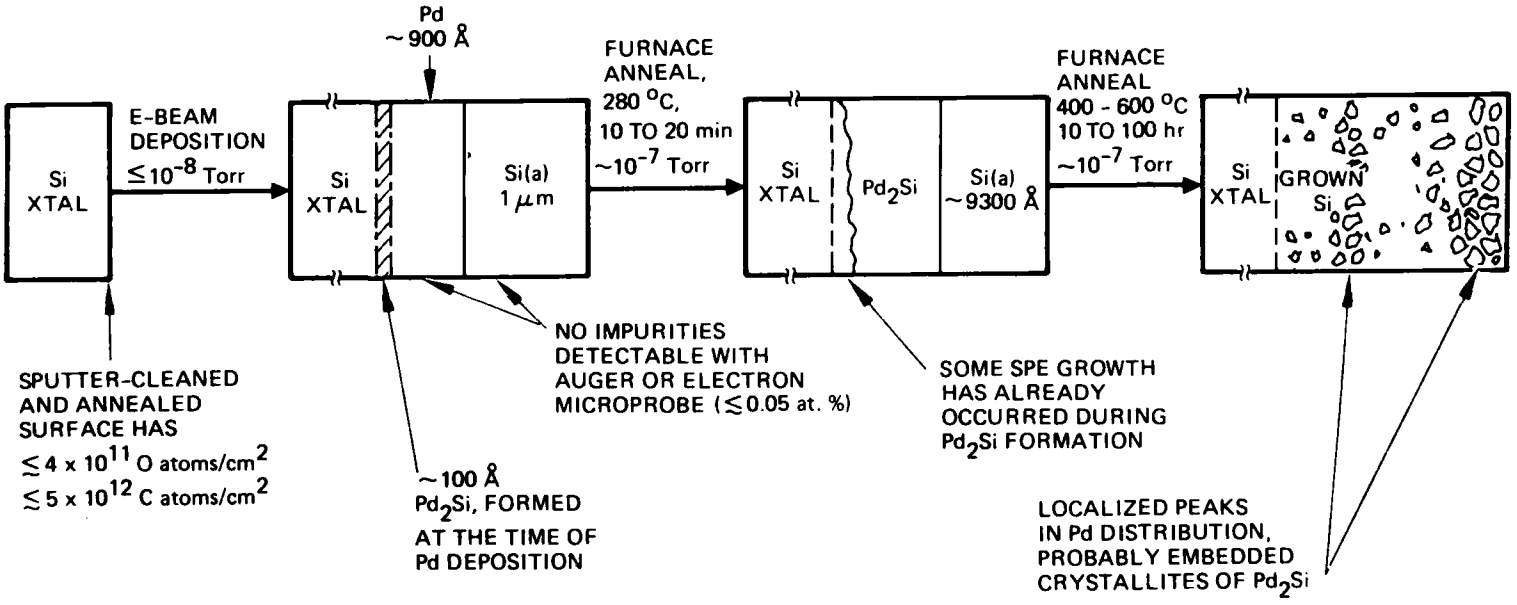


Figure 15. Depiction of Pd_2Si-interlayer SPE process showing behavior of non-pre-silicided samples annealed in a vacuum furnace.

is carried out in UHV prior to removal of samples into room air, the result of subsequent air exposure and furnace annealing is essentially identical to the case of all-UHV processing discussed earlier. As shown by the RBS spectrum in Figure 11, Si grows epitaxially but penetrates the Pd_2Si layer, producing a columnar Si epitaxial structure in which the outer surface contains a laterally inhomogeneous mixture of Si and Pd_2Si regions. From this result, therefore, and its comparison to the case where silicide is formed after air-exposure, we conclude that the outcome of Pd_2Si-interlayer SPE depends primarily on the properties of the silicide layer or silicide/Si(a) interface, and that these properties are somehow affected by air exposure of a sample prior to the silicide reaction. Of course, this implies also that the amorphous Si film itself is penetrable by room-air gaseous species, since it should otherwise prevent foreign atoms from reaching either the interface or the silicide.

Based on these observations, we examined the possibility of foreign atom penetration into deposited amorphous Si films. This work, which is discussed in detail in Section 4, showed that the low-density regions, or voids, present in deposited amorphous Si films[16-18] permit oxygen and carbon from the room-air ambient to diffuse rapidly into such films, producing concentrations as high as 0.1 to 1.0% and extending to depths as great as several thousand Angstroms. We considered that in silicide-interlayer SPE, the foreign atoms are either incorporated into the Pd_2Si when it is formed or are rejected by the silicide and collect at the Pd_2Si/Si(a) interface. However, Auger depth profiling failed to find any enhancement in oxygen concentration at the Pd_2Si/Si(a) interface, which argues against the rejection of O by the silicide and supports the incorporation of O within the Pd_2Si. Carbon, on the other hand, could not be profiled in regions containing Pd due to the overlap of C and Pd Auger peaks. Thus we could not determine the location of C in our samples directly. However, the Caltech group has obtained depth profiles of C in similar samples by using secondary ion mass spectrometry (SIMS) and

failed to find a C peak at the Pd_2Si interface[19]. It thus appears that both C and O are somehow incorporated into the Pd_2Si when it is formed rather than accumulating at the interface. The difference in the behavior of samples in which Pd_2Si is formed before or after exposure to room air must then be explained on the basis of contaminant effects on the silicide itself.

We can summarize the above-mentioned results on Pd_2Si-interlayer SPE as follows. When the silicide is free of contaminants, it breaks up during subsequent Si transport. Furthermore, if the silicide is contaminated with both C and O as a result of its being formed from air-exposed amorphous Si, then it not only will break up during transport, but also a large fraction of silicide will remain embedded far below the surface. Only if the silicide is formed from heavily carbon-contaminated amorphous Si will it remain continuous during transport to the surface in subsequent SPE.

These observations suggest that C and O affect interlayer-SPE in different ways and that C alone is necessary to achieve uniform layer transport. Specifically, it appears that oxygen in the amorphous Si can cause a barrier to silicide movement, possibly through the formation of SiO_2. However, this effect, which results in subsurface trapping of Pd_2Si, can be prevented entirely by incorporating a high concentration of C into the amorphous Si during deposition. To explain this, we hypothesize that the co-deposited C saturates the voids and thereby prohibits O absorption during subsequent exposure to air.

The remaining question is how C also prevents the silicide fragmentation observed in clean specimens. One possibility is that C reduces the SPE growth rate,[6] thereby allowing additional time for the silicide to reform into a continuous layer after it has been perturbed. Alternatively, the C may actually strengthen the Pd_2Si, perhaps by filling grain boundaries. Since the concentration of C incorporated during Si(a) deposition can be much higher (>1%) than that due to absorption of atmospheric gases (<0.1%), the silicide formed from a film contaminated during deposition could be significantly different. Although we know of no direct evidence on the effect of C on the mechanical properties and grain structure of silicides, it seems a subject worthy of future investigation.

It should be clear from the foregoing discussion that the mechanism of SPE using Pd_2Si interlayers is still not completely understood. We have shown clearly, however, that there is little promise in using the silicide-interlayer process for growing epitaxial films suitable for electronic device fabrication since, in all cases examined, the layers grown contained intolerably high ($\sim$0.1%) concentrations of Pd. Moreover, contrary to our initial expectations, the elimination of process-induced contaminants did not improve the quality of the epitaxial film in any practical sense. Instead, the growth morphology in pure samples was so different from that of C-contaminated films that the contaminated specimens would be preferable for practical applications. The most important result of our work, therefore, is probably the finding that silicide interlayers need not be used at all if the processing can be conducted in a contaminant-free environment, such as UHV. The experimental evidence supporting this contention is presented in Section 4, where we discuss the behavior and properties of "direct" (no-interlayer) SPE.

B. STUDIES OF Pd_2Si

During our investigation of silicide-interlayer SPE, we discovered some interesting properties of Pd_2Si that had not previously been reported. These include the observation of a LEED pattern from the surface of Pd_2Si grown on Si<111> and the formation of a Si skin on Pd_2Si and other silicides during heating in UHV.

We found that Pd metal deposited onto Si assumes a polycrystalline structure with a preferred orientation. This is evident in the X-ray diffraction data in Figures 16 and 17 taken on 2500 Å films deposited in UHV. The strong diffraction peak labelled Pd<111> in each of the figures is indicative of alignment of the <111> axes of individual Pd crystallites along the surface normal. The presence of a small amount of Pd_2Si that formed at the time of deposition is also evident.

Diffraction spectra taken after the samples were annealed at 400°C for 30 min in flowing argon gas are also shown in Figures 16 and 17. The presence of a strongly oriented Pd_2Si phase on the <111> substrate is clearly indicated by the large peaks labeled Pd_2Si. The d-spacing of the diffracting planes, 1.735 Å, is only in fair agreement with the 1.718 Å

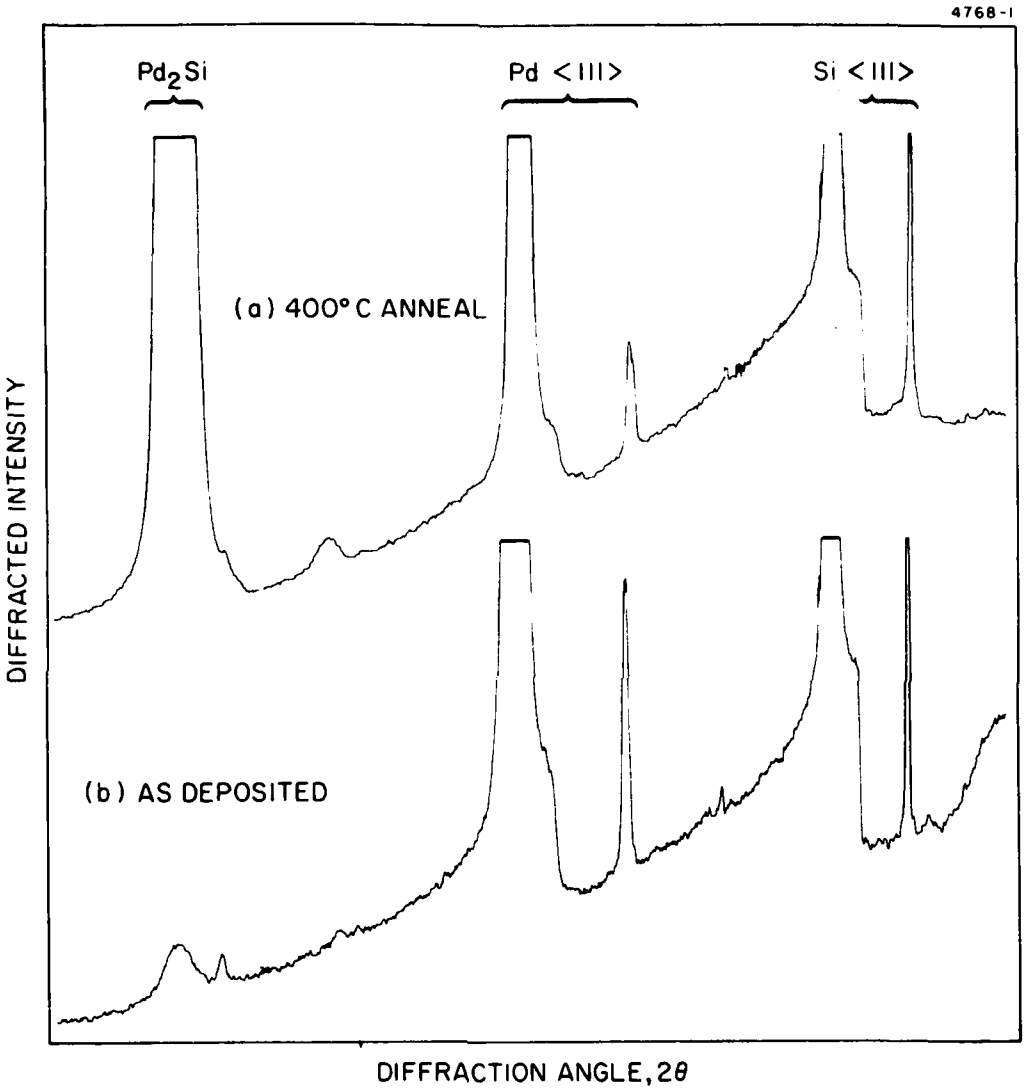


Figure 16. X-ray-diffraction spectra of UHV-deposited Pd on Si(100) before and after annealing for silicide formation.

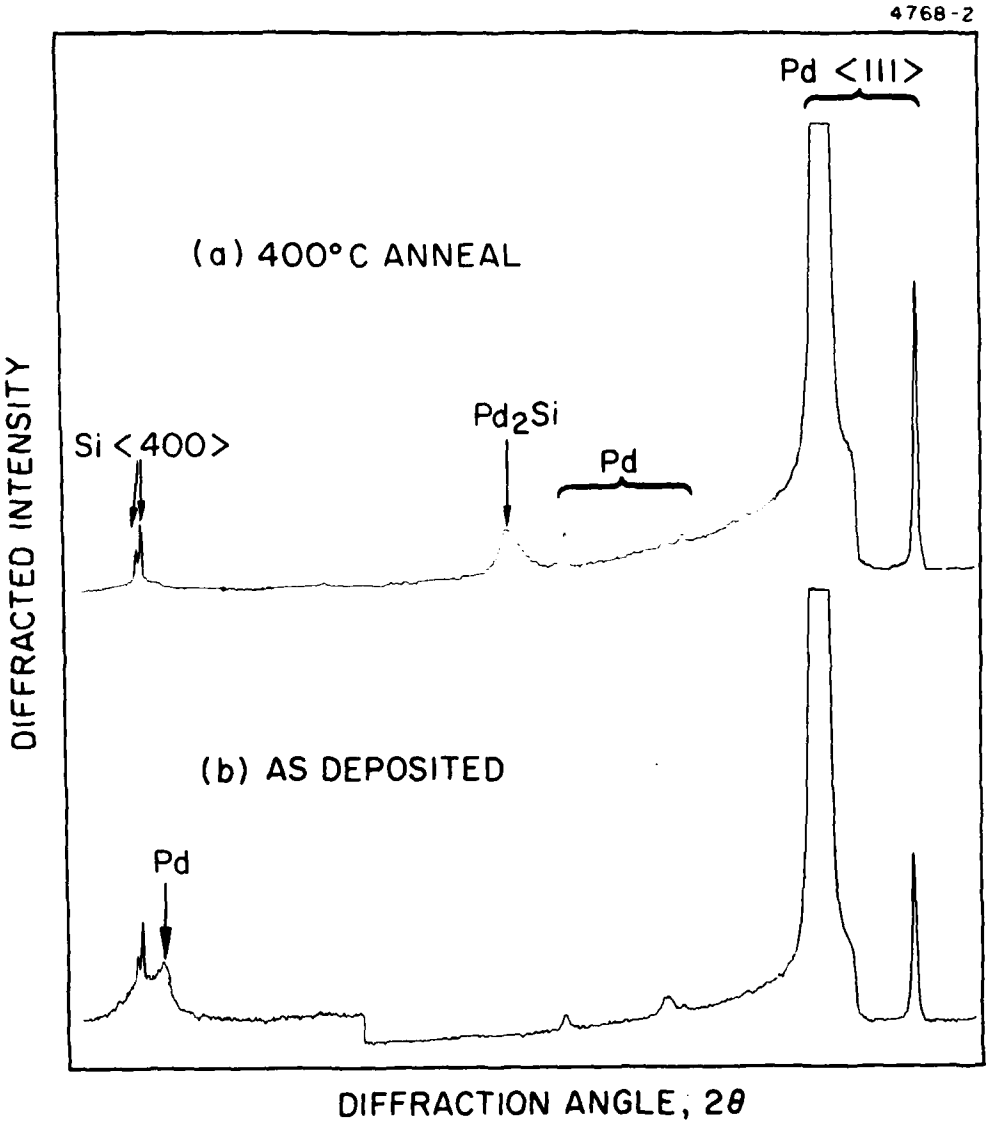


Figure 17. X-ray diffraction spectra of UHV-deposited Pd on Si(111) before and after annealing for silicide formation.

value for the 0016 planes of the 288 H^1 structure of Pd_2Si (ASTM 19-893) and the 1.71 Å value for the 002 planes of the 9H structure (ASTM 6-559). This variation from the standard values may be the result of strain produced by the significant amount of unreacted Pd in the film. The relatively incomplete comsumption of the initial Pd is probably the result of unavoidable contamination of the film during the period required to perform the X-ray analysis between film deposition and annealing. In the case of the <100> substrate, only a small, asymmetric peak is evident. This does not mean that the Pd_2Si phase failed to form; the formation of Pd_2Si is indicated by the reduction in size of all the Pd diffraction peaks. Instead, it indicates that the Pd_2Si phase formed on the <100> sample is less strongly aligned than that on the <111> sample. These results are consistent with the analysis by Buckley and Moss[20] which indicated that the 288 H^1 structure of Pd_2Si exhibits an excellent structural match with the <111> Si surface, and, in fact, tends to grow epitaxially on it.

The epitaxial nature of Pd_2Si formed on Si<111> has also been detected by LEED measurements made in UHV. Because the UHV environment makes it possible to form the silicide with an atomically clean surface, it is possible to observe electron diffraction from the outermost atomic layers. The LEED pattern generated by a freshly formed <111> Pd_2Si surface was found to be in registry with that from the Si<111> substrate, indicating an epitaxial structure. However, the silicide LEED pattern was complex and required for its description the assumption of two types of crystallographic domains rotated by 30° relative to each other. The existence of two domains in Pd_2Si is not surprising since it can be seen from the model of Buckley and Moss[20] that alternate atomic layers have primitive translation vectors rotated relative to each other by 30°. Thus, the two domains suggested by the LEED pattern probably consist of adjacent regions in which the extent of silicide formation differs by an odd number of atomic layers.

In addition to observation of an ordered surface on Pd_2Si, we also discovered that, after prolonged heating, the surfaces of Pd and Pt silicides become covered with a thin Si skin. Evidence for this is presented in Figures 18 and 19, which show the results of Auger depth-profiling of Pd_2Si samples prepared in UHV. The upper panel of Figure 18 shows a silicide formed by 10 min heating at 400°C at a pressure less than 10^{-7} Pa. Only the Si and Pd concentrations are given since no impurities whatsoever were detected on the UHV-formed samples. In Figure 18(a) only a slight indication of Si enrichment at the outer surface of the film is evident. The skin is only partially developed because of the short annealing time and low temperature employed. In contrast, the lower panel of the figure shows a greatly expanded depth-profile of a well-developed Si skin formed by 500°C heating in UHV.

Additional annealing beyond the conditions of Figure 18(b) does not cause any significant further Si accumulation, suggesting that there is an equilibrium thickness for the skin. Accounting for the attenuating effect of the Si skin on Auger electrons emitted from the underlying silicide, we have calculated an approximate thickness of about 6 Å for the fully developed skin on Pd_2Si. This same thickness is found for Pd_2Si formed on both <100>- and <111>-oriented substrates, consistent with the fact that the orientation of the Pd_2Si itself is independent of the substrate.

A Si skin has also been found on PtSi and $NbSi_2$ after annealing. The generality of the phenomenon suggests that a Si-covered surface is the thermodynamically favored condition for most silicides. This hypothesis is further supported by our observation that the Si skin can be sputtered off but readily forms again upon subsequent heating. This thermal regeneration is illustrated in Figure 19 for Pd_2Si.

The ease with which a Si-rich surface forms on transition metal silicides may explain why a silicon-oxide layer is always observed on the surface of silicide films exposed to air and on silicides reacted in non-UHV environments. Auger depth-profiling has shown that a SiO_2

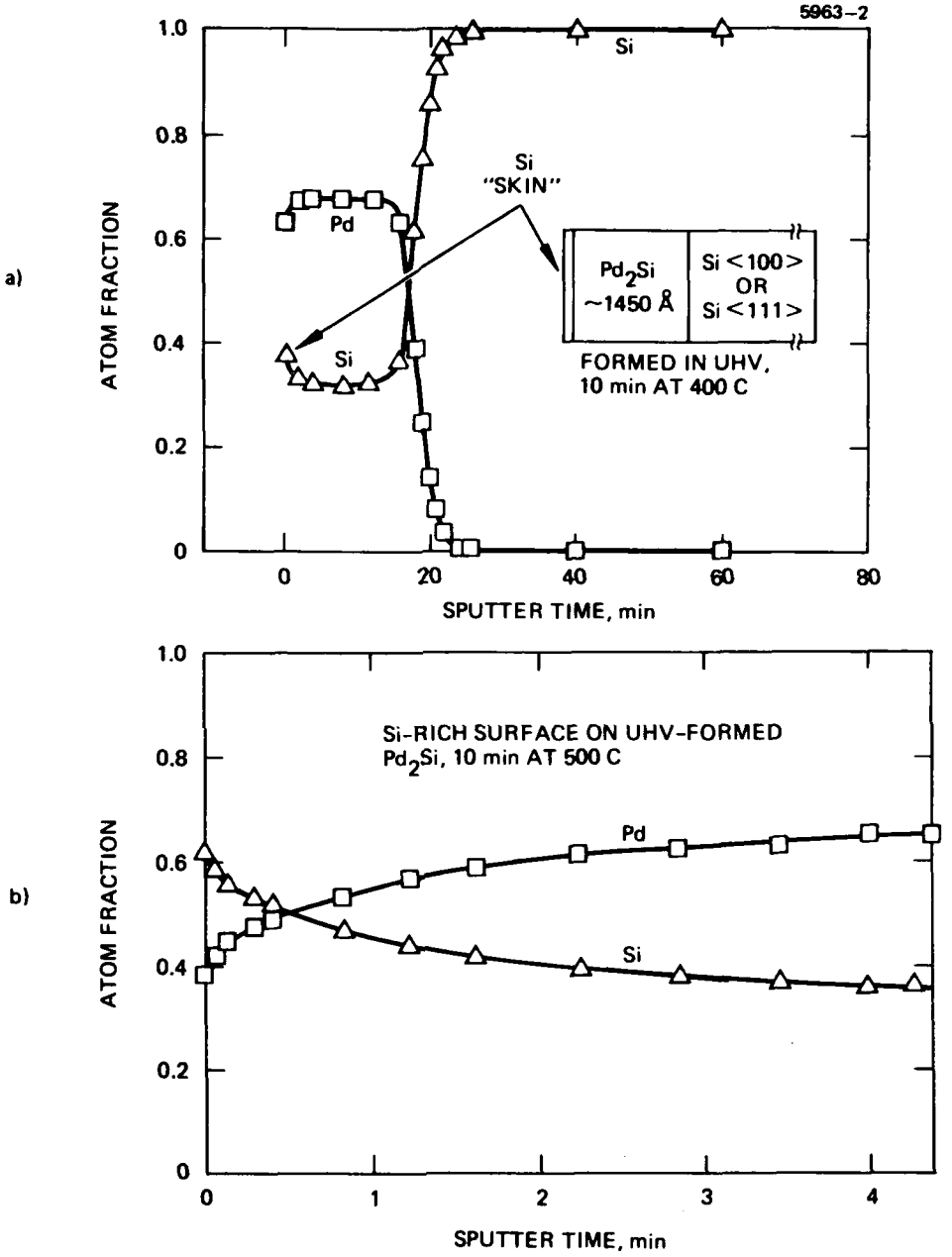


Figure 18. AES depth profiles of Pd and Si concentrations in Pd_2Si formed in UHV by heating for: (a) 10 min at 400°C; (b) 10 min at 500°C.

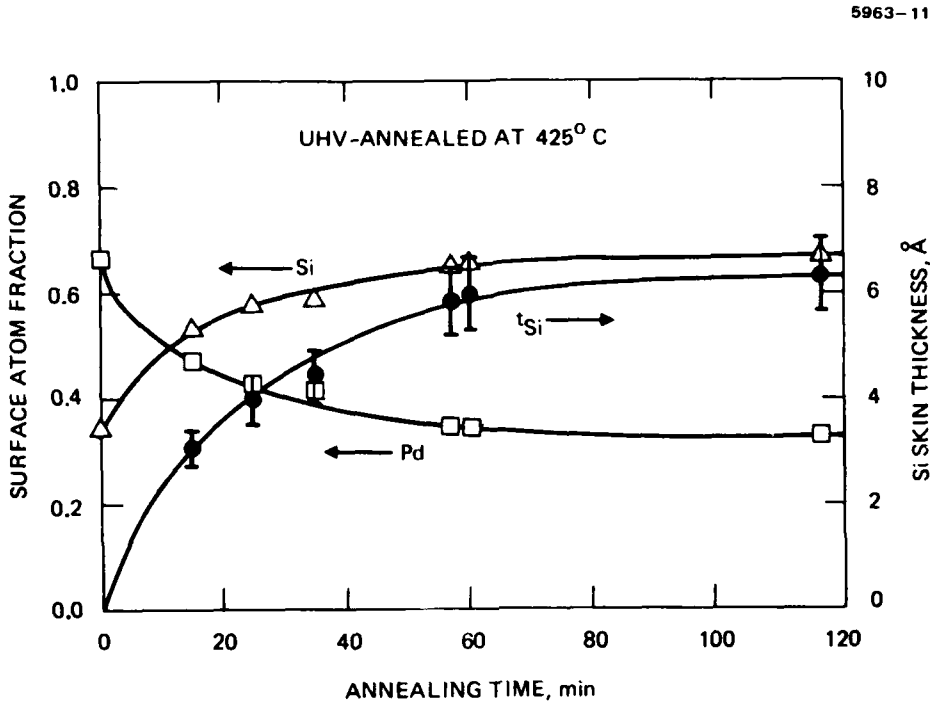


Figure 19. Thermal regeneration of the Si skin on Pd_2Si.

surface layer is always present on Pd_2Si reacted in a vacuum furnace, even when the Pd deposition was carried out in UHV on an atomically clean substrate and in situ examination failed to find any oxygen within the film. In the case of Pd_2Si, oxide forms even during annealing in a high-vacuum furnace ($<2 \times 10^{-4}$ Pa) and it must be etched off before aqua regia will attack the underlying silicide. Evidently, the rapid migration of Si through the silicide supplies excess Si to the outer surface, which then reacts with oxygen present in the furnace ambient.

SECTION 4

DIRECT SPE OF DEPOSITED FILMS

We investigated the direct SPE of Si films deposited onto Si single-crystal substrates. This work divided naturally into two parts. First, we studied "intrinsic" SPE by performing all the processing (such as substate cleaning, film deposition, heating, and diagnostics) in UHV. Then we relaxed the processing conditions in order to examine some of the effects of contaminants.

This section begins by reviewing the processing we employed for contaminant free or intrinsic SPE in UHV. Then the results of studies of the film properties (e.g., crystallographic defects, substrate orientation dependence, dopant incorporation) are presented and the electrical behavior of transistors made in SPE material is discussed.

The study of contaminant effects is discussed with reference to two principal issues: (1) substrate cleanliness and its effect on defects in the epitaxial layer and (2) the effects of exposure to room air prior to SPE growth. It is shown that remarkably clean Si surfaces can be prepared by chemical cleaning prior to insertion into the UHV chamber, permitting some SPE growth even without in situ substrate preparation. However, even when substrate preparation and film deposition are conducted in UHV, subsequent exposure of an amorphous film to room air permits the in-diffusion of atmospheric gaseous species to a high concentration. These contaminants are shown to interfere with SPE and cause polycrystallization to occur. Contaminants are also expected to have a deleterious effect on the performance of electrical devices made in SPE material exposed to room air prior to growth. These observations imply that the entire SPE process should be carried out in UHV to obtain films of the highest quality.

A. PROCESSING USED FOR DIRECT SPE

The processing required to grow high-quality SPE films consisted of the steps indicated in Table 4. Pre-vacuum chemical cleaning was

Table 4. Process Used for Direct SPE

1.	Chemically clean substrates (cf. Table 2)
2.	Load 8 samples in UHV system
3.	Pumpdown and bakeout for 12 hr
4.	Degas UHV system components
5.	Sputter-etch ∿50 Å from surface using 2-kV Ar^+
6.	Anneal sputter damage: 850 to 950°C, 2 min
7.	Verify surface cleanliness and crystallinity with Auger and LEED
8.	E-beam deposit Si: ∿1 to 2 Å/sec
9.	Heat to ∿550°C using radiant disc, to induce SPE
10.	Verify growth complete using LEED

found not to be particularly critical, provided that gross organic contamination was prevented, because subsequent UHV sputter-etching could readily remove up to 50Å of material from the surface. However, for large samples, such as 2-in.-diameter wafers, the sputter-etching beam current density was rather low, requiring etching times of several hours for significant material removal. Consequently, for large samples it was advantageous to use careful chemical cleaning procedures to minimize the required UHV etching time. The process detailed in Table 2 was found to be very satisfactory for this purpose.

In situ surface cleaning was performed by sputter-etching with 2-keV Ar ions from an ion gun directed at the surface, inclined to give an incidence angle approximately 10 to 20° off the surface normal. This procedure minimized deep penetration of the incident ions and prevented the Ar trapping effects experienced by other workers.[21] Using this technique, it was possible to achieve a degree of surface cleanliness as evidenced by AES such that the surface concentration of foreign species was less than 0.1% monolayer.

Post-sputter annealing for expulsion of embedded Ar and restoration of surface long-range order was performed by heating the sample with a radiant disk (cf. Section 2). An annealing temperature above about 750°C was necessary to expel the Ar and produce satisfactory surface re-ordering as judged by existence of a LEED pattern. Actual LEED contrast depended on the temperature used, being superior for higher temperatures. However, we held the annealing temperature below about 950°C because higher temperatures caused a pressure rise and resulted in re-adsorption of impurities and degradation of the LEED pattern. We were unable to establish a clear connection between post-sputter annealing temperature and defect structure of epitaxial films grown by SPE. However, it is likely that the density of crystallographic defects near the substrate/film interface could be reduced if higher temperatures could be used without producing re-contamination.

Deposition of amorphous Si was performed by E-beam evaporation with no hearth liner in the crucible in order to reduce the possibility of

contaminant introduction into the films. Moreover, the Si source material was only melted in its center so that the melt did not touch the crucible. This latter precaution had the effect of limiting the deposition rate of Si to less than about 2 Å/sec. Consequently, it was impractical to study the effects of deposition rate on defect densities in SPE films because of the long deposition times required. However, we did determine that, for films which are exposed to room air prior to SPE growth, higher deposition rates are desirable. This point is discussed later in this chapter.

SPE growth was induced by heating within the UHV chamber with the same radiant heater employed for annealing sputter damage. Growth temperatures between 500 and 600°C were typically used since the resulting growth rates permitted complete conversion of films several thousand Angstroms thick in times of several hours or less.

The upper limit of SPE growth temperature was established primarily by the fact that, for temperatures above about 750°C, the sample temperature could not be raised quickly enough to ensure that most of the growth occurred at the final steady-state temperature. Recently, however, we implemented the capability to conduct SPE at high temperatures by the use of laser irradiation in the UHV chamber. The rate of temperature rise using cw laser irradiation is sufficient to permit SPE growth to be conducted at over 1100°C.

It was generally quite simple to verify that SPE growth had occurred throughout the film because of the difference in reflectivity between amorphous and crystalline Si. Usually, the initially silver-colored amorphous film would first become darker in one localized spot corresponding to the location of highest temperature on the disk heater. Then, with further annealing time, the darker epitaxial region would expand laterally. Just beyond the perimeter of the dark region it was possible to observe fringes of different colors caused by optical interference between light reflected from the surface of the remaining amorphous film and light reflected from the crystal/amorphous interface.

LEED was used to verify that the color change from silver to dark observed visually was in fact representative of epitaxial crystallization.

It was generally found that the quality of the LEED pattern (viz. contrast and spot definition) from a grown film was superior to that from the substrate. In fact, we often observed 1/4-order diffraction spots from the Si<100> surface of an SPE film, whereas they were only occasionally seen on sputter-cleaned and annealed wafers. According to the atomic diffraction work of Cardillo,[22] we can assume that 1/4 order diffraction beams are an intrinsic feature of the reconstructed Si<100> surface, and that their occurrence therefore indicates a high-quality surface condition.

In situ Auger spectroscopy on SPE-grown layers failed to detect any contaminants at the outer surface or within the epitaxial films. Thus, any contaminants incorporated into the Si film during deposition or prior to SPE apparently do not segregate at the crystal/amorphous interface, or else are present in low enough concentrations that such segregation is undetectable by AES.

B. DIRECT SPE WITHOUT CONTAMINANTS

We turn now to a discussion of the properties of epitaxial layers of Si grown by direct SPE of deposited films in UHV. An indication of the degree of crystallographic perfection of SPE films was obtained by transmission electron microscopy (TEM) and Rutherford backscattering (RBS) channeling-effect analysis. Figure 20 presents RBS channeling spectra showing epitaxial crystallization of a 4500-Å Si layer on <100> Si induced by heating for 2 hr at 525 ± 25°C. The 25:1 reduction in backscattered yield after growth is strong evidence for high-quality epitaxy. Indeed, the channeling spectrum of the film in Figure 20 is indistinguishable from the corresponding spectrum taken on an exposed portion of the single-crystal substrate on this sample. Thus, RBS indicates that a high-quality epitaxial film has been grown.

TEM was employed to obtain a more definitive determination of the crystallographic perfection of SPE films. Figure 21 shows a bright-field micrograph from a typical area on a <100> Si SPE layer along with the corresponding selected-area diffraction pattern. The micrograph shows no planar defects such as stacking faults or twins. The absence

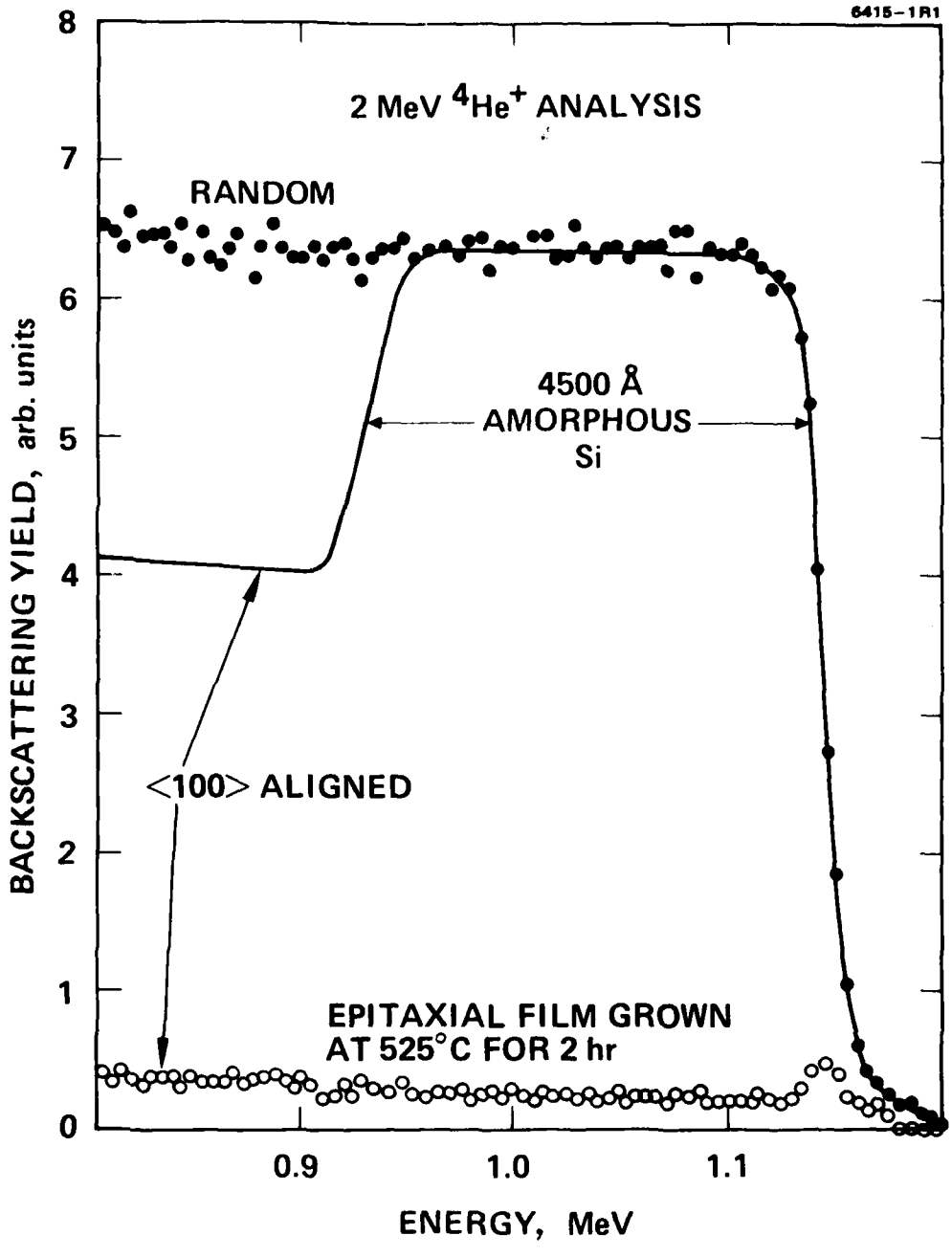


Figure 20. Channeling spectra showing SPE conversion of an initially amorphous 4500-A Si film (solid line) into an epitaxial single-crystal layer (open circles).

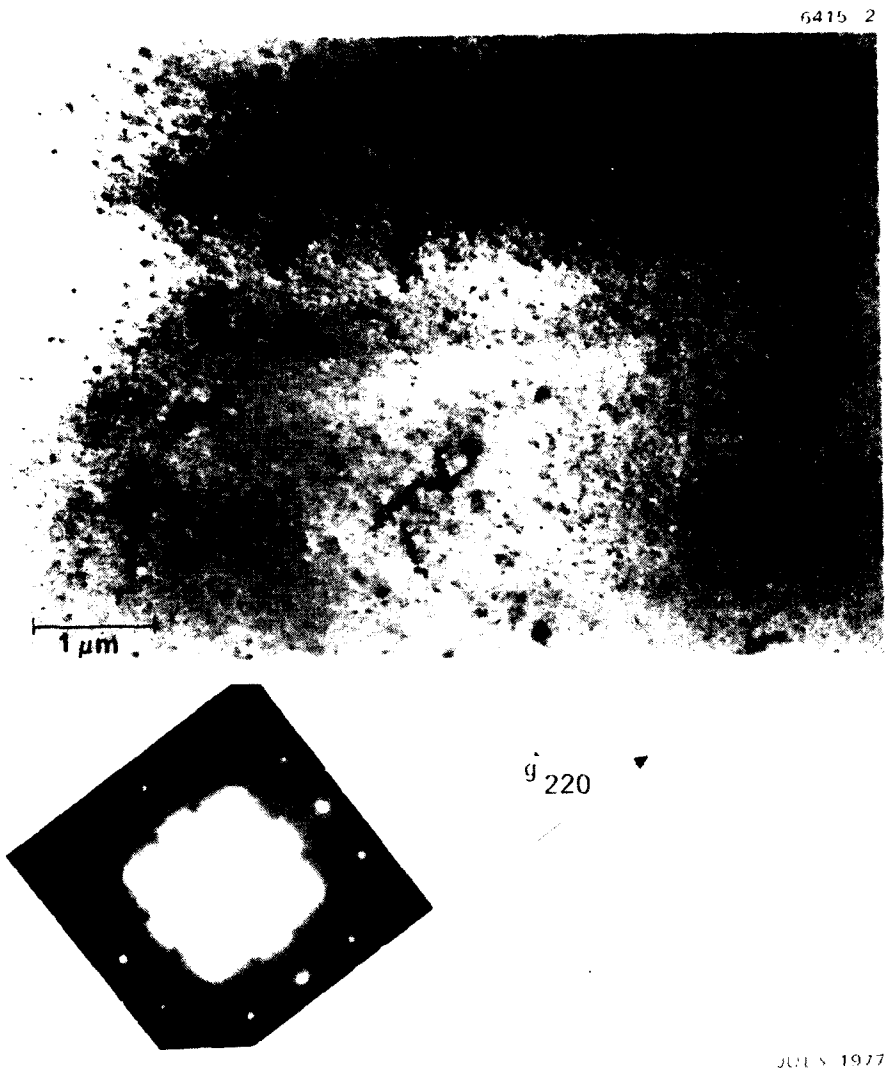


Figure 21. Bright-field transmission electron micrograph of a 4500-Å Si(100) film grown by SPE at 525°C.

of such defects was confirmed by examining micrographs taken under several different diffraction conditions. It is known that planar defects arise primarily from substrate contamination,[23] so their absence in the present samples is probably attributable to the excellent substrate cleanliness achieved by sputter-etching and annealing in UHV. Figure 21 does show, however, the presence of several groups of straight dislocations of approximately equal length as well as a high density of very small, dark features. Detailed examination of the dislocation images has shown that they originate at or near the substrate/film interface and extend through the epitaxial layer, inclined relative to the surface normal. This type of behavior, which is suggestive of defect generation at the site of substrate imperfections, may indicate that the sputter-anneal procedure is not wholly effective in generating a perfect substrate surface.

This hypothesis is supported by the results of further TEM analysis which shows that the defect density in SPE films decreases toward the surface. Figure 22 contains bright-field micrographs taken on a 1-μm-thick SPE layer on <100> Si. The lower panel of Figure 22 is a projection through the entire layer, whereas the upper panel shows only the outer 2000 to 3000 Å. This comparison shows clearly that the defect density is far less in the outer portion of the epitaxial layer.

Films as thick as 2 μm have been grown by SPE, and although we have not performed TEM on the thickest films, RBS channeling analysis has shown that the crystal quality remains excellent throughout the range of thicknesses from 2000 Å to 2 μm. Since the surface of an SPE film is more perfect than that of the original substrate, multiple layers grown sequentially on top of each other exhibit good crystallinity. In fact, as is also the case in MBE, the best films are grown when an SPE buffer layer is used as the substrate for further epitaxy.

Although epitaxial films of excellent quality can be grown on <100>-oriented Si substrates, this is not necessarily true for other substrate orientations. On <111> Si, for example, SPE produces a highly defect-laden film, as indicated by the comparison of RBS channeling

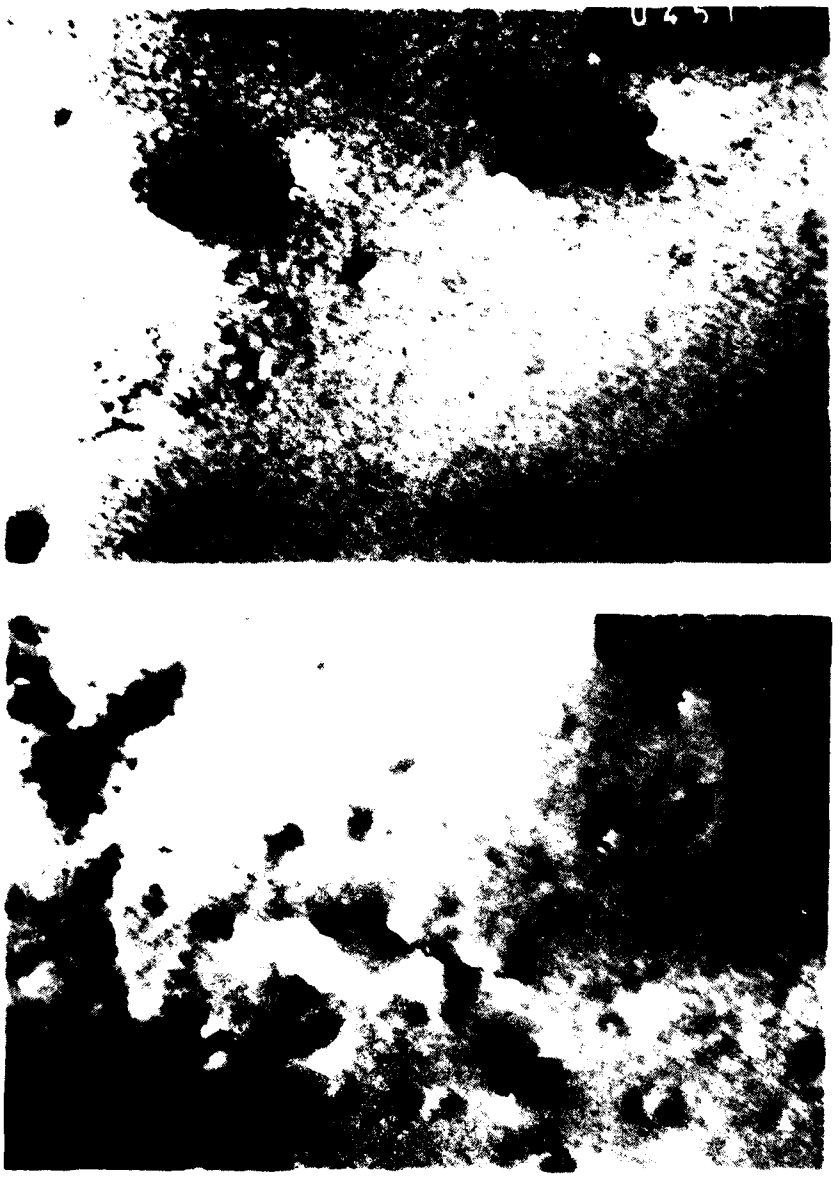


Figure 22. [illegible] film containing [illegible] 5000 Å (upper panel) [illegible] the entire [illegible].

spectra in Figure 23. The <111> film exhibits poor channeling. Although we did not perform TEM on <111> Si SPE, we can draw some conclusions about growth on this orientation from the analogous work on recrystallization of ion-implanted amorphous films[24]. There it was found that, on <111> Si, a high density of microtwins forms during SPE crystallization. It has also been observed that the SPE growth rate on <111> Si is very much lower than on <100> Si[24]. It was suggested that the lower growth rate and high defect density are both manifestations of the fact that SPE on <111> Si can only proceed by localized nucleation and island growth[25] instead of the planar growth mode hypothesized for <100> oriented material.

We were not able to directly measure the growth kinetics on films grown in UHV because of the difficulty of determining the growth temperature accurately. Attachment of a thermocouple directly to the sample is impractical because of the many degrees of motional freedom required to carry out the process in UHV. The common practice of making good thermal contact between the sample and its holder, then reading a thermocouple attached to the holder could not be used because of the difficulty of making good thermal contact in UHV without stressing the wafer. Stress is undesirable because during heating it is relieved by dislocation generation, which can produce massive concentrations of dislocation networks, or "slip planes."

The growth kinetics of SPE in deposited films cannot be studied by removing samples to a furnace for controlled heating, as has been done for implanted layers.[24] Later, we show that deposited amorphous Si films absorb large quantities of oxygen and carbon when exposed to room air. These impurities are known to alter the growth kinetics.[26] Thus, although kinetics could have been measured using the RBS channeling effect, the growth rates measured would not have been the intrinsic rates for uncontaminated films.

Since we could not directly determine the SPE rate for deposited films, we assumed that data measured on implants are appropriate.

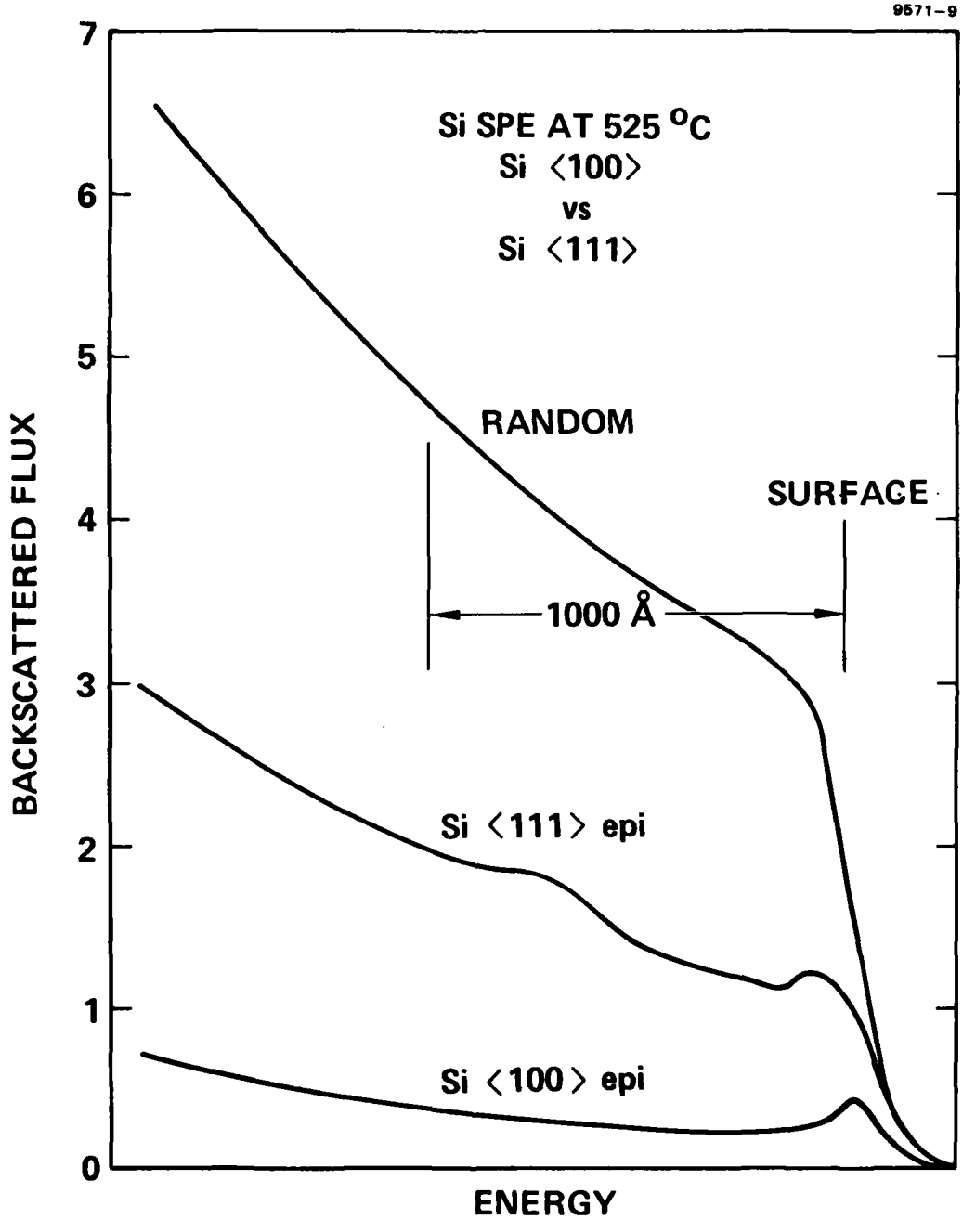


Figure 23. RBS channeling spectra comparing SPE on <100>-oriented and <111>- oriented Si substrates.

Cspregi et al.[27] found that for <100> Si the SPE rate varies with temperature as:

$$R(\mathring{A}/s) = 3.17 \times 10^{14}\ e^{-2.35\ eV/kT}\ .$$

This dependence is plotted in Figure 24 for reference. The ±25°C uncertainty in our UHV temperature measurements allows for nearly a factor of 80 difference in growth rate, so any kinetics data obtained in UHV would be meaningless. Therefore, we can only state that, in general, the time required to grow a particular film seemed to follow the predictions of Figure 24.

Besides the dramatic effect of temperature on the growth rate in SPE, it is possible that the microstructure of the grown films may also depend on the temperature employed. This issue has not been adequately addressed because of the difficulty of conducting SPE at temperatures much above 600°C by conventional heating methods. According to the growth rate data presented in Figure 24, the rate increases so rapidly that one has to be concerned with the rate of temperature rise during the initial heating of a sample. If, for example, the temperature of the sample rises 50°C/sec, a typical rate for oven annealing, then it is meaningless to attempt to grow at temperatures much in excess of 750°C since most of the film would be converted before the temperature reached its steady-state value. In a practical sense, the only way to achieve the rapid heating rates necessary to reach effective temperatures above 1000°C is by the use of laser or electron beam irradiation. Using a scanned cw Ar ion laser, for example, at a scan velocity of 3 cm/sec, it is possible to reach effective SPE temperatures of up to 1200°C.

SPE films grown at high temperature in the UHV chamber using Ar laser irradiation[28] have been examined with RBS channeling and found to exhibit channeling yields identical to the best layers grown at lower temperatures. However, TEM has not yet been performed, so we do not know whether the higher temperature affects the microstructure in a more subtle way than can be detected by RBS.

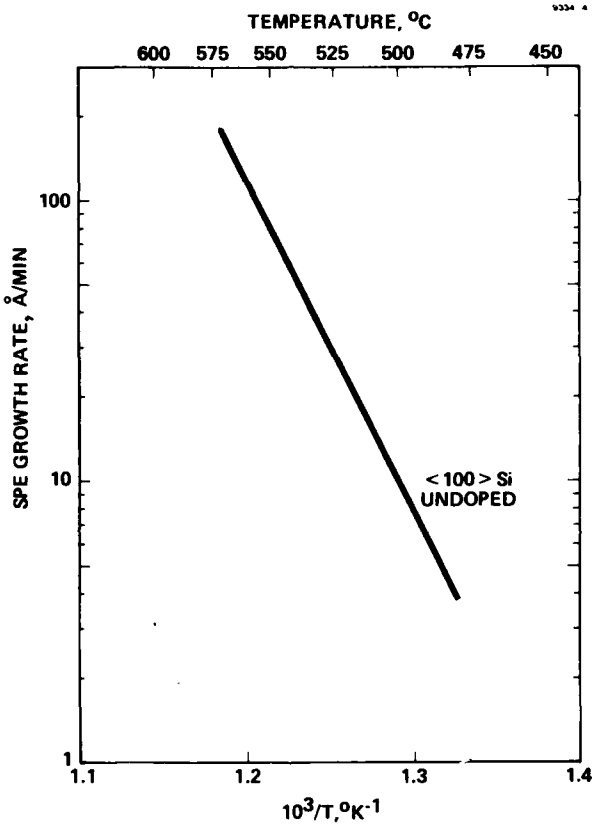


Figure 24.
SPE growth rate for ion-implanted amorphous Si layers on <100> Si (Reference 27).

It is possible that a practical upper limit exists for the temperature and film thickness which can be employed in SPE before random nucleation of crystallites begins to become a problem. Blum and Feldman[29] have studied the amorphous-to-polycrystalline conversion of Si films and concluded that, in the temperature range from 560 to 700°C, the time to convert 95% of a film to poly is given by:

$$\tau(s) = 1.02 \times 10^{-13} e^{3.1\ eV/kT} .$$

If this expression is valid at temperatures greater than 700°C, then a 3-μm-thick film heated to 1000°C would be 95% poly at its outer surface after heating. Consequently, according to this argument, thick films should not be grown at high temperatures. In practice, one would probably want to ensure that the fraction of a film subject to amorphous-to-polycrystalline conversion be less than a given value. Then, it is not appropriate to use Blum and Feldman's results since they did not determine the dynamics of poly formation, only the time to reach 95% conversion. Koster[30] followed the amorphous-to-poly conversion in an electron microscope and found that the number of randomly oriented crystallites formed per unit volume per sec exhibits an "onset" or delay time that decreases with increasing temperature. At 647°C, for example, essentially no crystallites form for the first 1000 sec. Therefore, in SPE at 647°C, a film as thick as 4.16 μm could be grown without significant poly formation. Both Blum and Feldman[29] and Koster[30] concluded that the time to convert a fixed fraction of a film to poly decreases exponentially with increasing temperature with about a 3.1- to 3.3-eV activation energy. In comparison, the time to epitaxially crystallize a film of given thickness decreases exponentially with a 2.35-eV activation energy.[27] Therefore, if these temperature dependences also hold for higher temperature, amorphous-to-poly conversion will become increasingly competitive with SPE as the temperature is increased. However, Koster has suggested that the steady-state nucleation rate for poly formation will reach a maximum near 850°C and then

decrease as temperature increases. If this is the case, high temperatures would be more favorable for SPE.

C. BEHAVIOR OF DOPANTS IN SPE

Because of the low temperatures possible in SPE, dopant atoms should not diffuse significantly during growth. This makes SPE an attractive substitute for other forms of Si epitaxy (such as CVD), where the high temperatures employed cause significant dopant redistribution.

Figure 25 shows that, even when an undoped SPE film is grown on a heavily doped substrate, the substrate dopant atoms do not penetrate into the epitaxial layer. The SIMS depth profile of Sb in three SPE films of different thicknesses grown on the same substrate show very abrupt film/substrate boundaries. The Sb profiles are rounded slightly by the roughening effect of the ion-etching used in SIMS, an effect that increases for deeper profiles. The Sb profile in a film grown by conventional CVD at 980°C is offered for comparison.

There are several methods possible for introducing dopants into an SPE film; however, the most convenient is to co-deposit the dopant along with Si to form a doped amorphous Si film which can then be converted to epitaxial by SPE. Presumably, since the substrate is at room temperature during deposition, all the dopant atoms would stick and be incorporated into the film. This would avoid one of the problems of doping in MBE, that of temperature-dependent sticking coefficients. However, it was not clear at the outset whether dopant atoms incorporated into an amorphous Si film would be incorporated onto lattice sites during SPE and thereby become electrically active. To answer this question, we grew films doped with boron by using a boron-doped Si source in the evaporator.

Figure 26 shows the boron atom concentration in an SPE layer grown on a lightly boron doped substrate. The boron concentration determined by SIMS varies somewhat through the film but achieves an average level of roughly $7 \times 10^{17}/cm^3$. The boron profile near the film/substrate

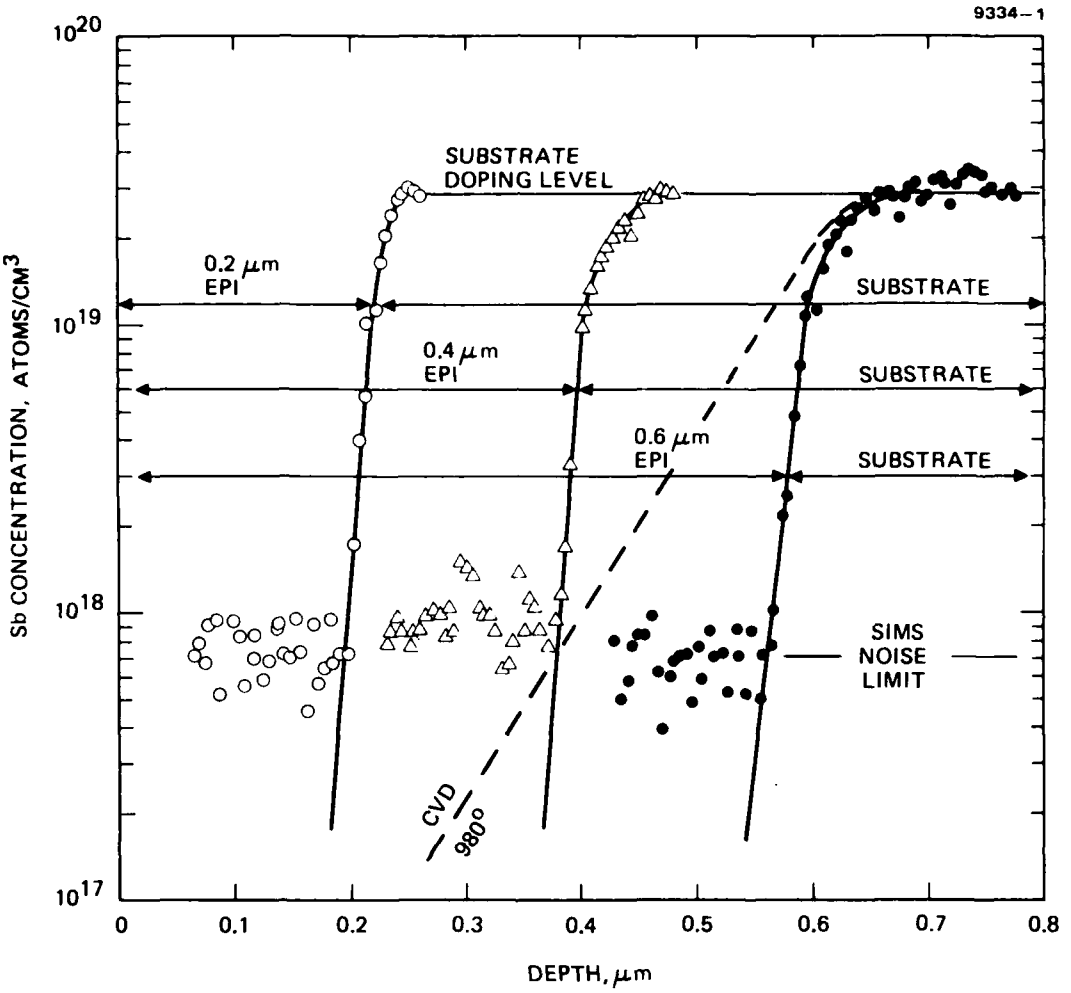


Figure 25. Antimony concentration depth profiles across the film/substrate interface in undoped SPE films of three different thicknesses grown on a Sb heavily doped substrate.

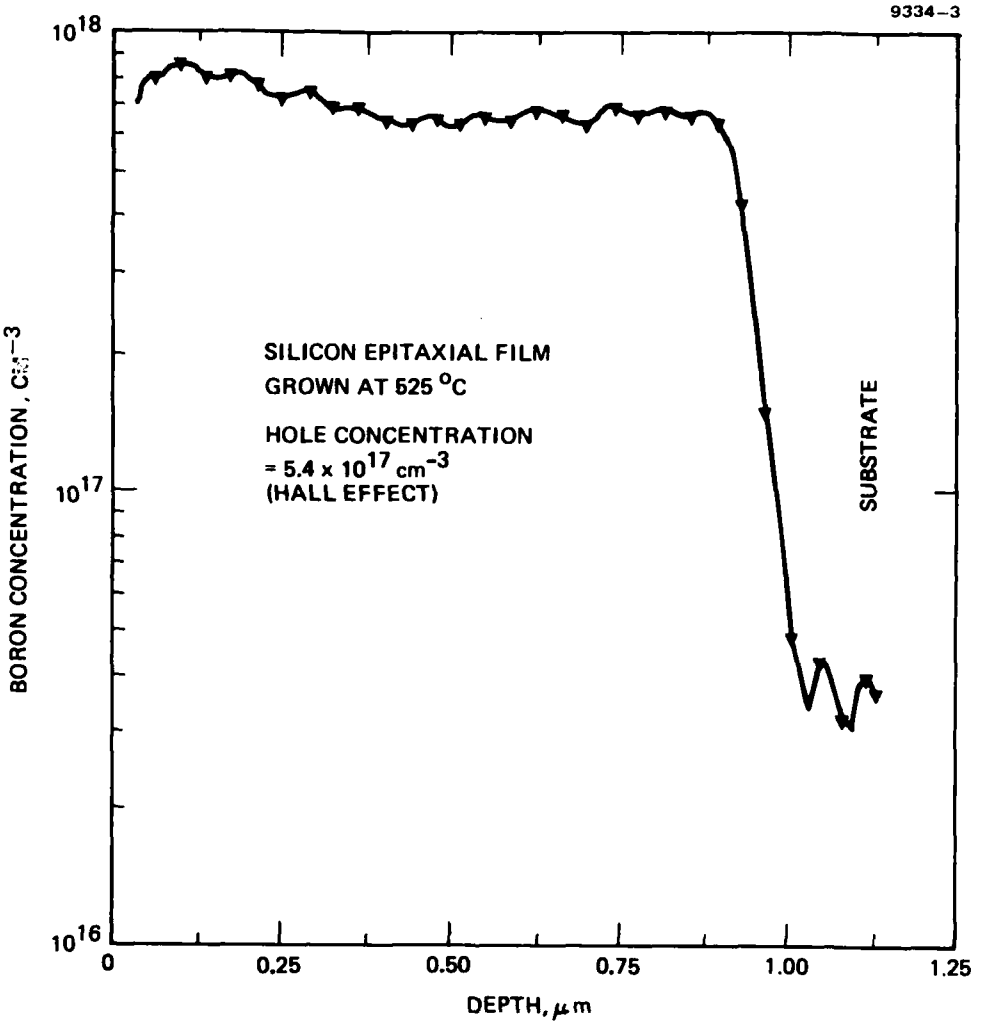


Figure 26. Boron concentration profile in a boron-doped SPE film grown on a lightly boron doped substrate.

interface is very abrupt, as expected. Hall effect measurements determined that the hole concentration in this film was about $5.4 \times 10^{17}/cm^3$. Thus, about 77% of the boron atoms are electrically active. Although this figure may be in error by as much as ± 20% because of the difficulty in calibrating SIMS, it nevertheless indicates a high activation efficiency for doping in SPE.

D. DEVICE FABRICATION

To further evaluate the electrical quality of SPE-grown Si and to test the suitability of SPE material for device fabrication, we made MOSFETs in layers grown on 2-in.-diameter Si wafers. SPE films about 7500-Å thick were grown on Si<100> substrates using our standard processing. No intentional doping was added since the dopant concentration could not be controlled to the degree required for MOSFET fabrication without adding a separate deposition source for the dopants. After SPE growth, the wafers were processed along with a batch of bulk Si wafers in the manner normally used at HRL to fabricate short-channel MOS circuits. Doping for source, channel, and drain regions was introduced by ion implantation. During processing, samples were heated to 925°C for oxidation, diffusion, and implant annealing.

Enhancement-mode n-channel MOSFETs fabricated in the SPE material were compared directly to control devices produced in the same run using standard bulk Si wafers as substrates. Typical transistor characteristics measured on an SPE FET having a 1.2-μm-long channel are shown in Figure 27. From these data as well as I-V characteristics of many other SPE-FETs having channel lengths up to 25 μm and widths from 2.5 to 100 μm, we determined that the electrical properties of devices formed in SPE Si are indistinguishable from their bulk counterparts. Channel mobilities ranged from 367 to 478 $cm^2/V\text{-sec}$, comparable to the bulk devices and consistent with the $2 \times 10^{17}/cm^3$ channel doping employed. MOS threshold voltages, breakdown voltages, and leakage rates for SPE-FETs also fell within the range of values observed on the control bulk devices.

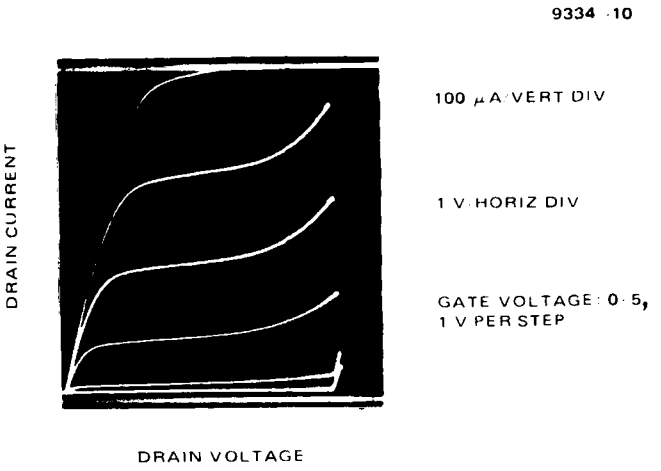


Figure 27.
Source-drain (I_d vs. V_d) characteristics of an enhancement-mode, n-channel MOSFET made in SPE-grown Si.

These results indicate that there is no intrinsic problem associated with the low growth temperature of SPE as far as electrical transport properties are concerned. Moreover, the Si/SiO_2 interface in oxidized SPE material apparently does not contain a high density of interface states since the MOS threshold voltages were comparable to those of the bulk devices. We believe that these results are compelling evidence for the suitability of SPE as a growth method for IC applications. However, it is important to conduct further tests (e.g., measuring the minority carrier lifetime and determining possible deep-level traps by DLTS) to arrive at a more detailed characterization of the electronic properties of SPE material.

E. CONTAMINANT EFFECTS ON DIRECT SPE

We studied two types of contaminant effects. We briefly examined the effect of substrate contamination on the properties of SPE films; the motivation was recent reports[31] that films can be grown directly on chemically cleaned substrates. A detailed study was conducted on the effects of exposing amorphous Si films to room air prior to attempting SPE.

It has generally been accepted that, regardless of the chemical etching procedure used, subsequent exposure of a Si wafer to room air will result in the growth of 5 to 15 Å of oxide on the surface.[32] In past studies, we confirmed this and found that bakeout of the UHV system further increased the surface coverage of oxygen- and carbon-containing species. In both our own initial work on SPE and that of others[3,4], it was found that the oxide and other adsorbed contaminants on Si prohibit direct SPE of deposited films unless in situ cleaning is used.

Recently, however, we have obtained results that are radically different from our earlier findings. Substantial improvements were made in the degree of surface cleanliness that can be achieved on Si by wet chemical processing alone. Using the cleaning procedure presented in Table 2, we found it possible to produce Si surfaces containing less than a monolayer of total adsorbed and C. A LEED pattern,

albeit one of poor quality, has been observed from such surfaces without any in situ treatment! To our knowledge, this is the first time that LEED has been observed on Si without in situ cleaning or cleavage of a crystal.

It is difficult to understand how a Si wafer removed from an etching solution can undergo exposure to room air without adsorbing at least one monolayer of oxygen-containing species. To rationalize our observations, therefore, we considered the possibility that after the final etch in HF the surface is mostly covered by an adsorbate layer that effectively passivates it against further adsorption. It is possible that either fluorine or hydrogen adsorbs in sufficient quantity to protect the surface during subsequent air exposure. However, using Auger spectroscopy, we were unable to detect fluorine on Si surfaces in UHV; so if F is the responsible species, it apparently desorbs in the vacuum environment. Hydrogen, on the other hand, is not detectable by Auger analysis, so it could be present on the surface. In fact, hydrogen is known to bond to the free Si surface[33] so it is reasonable to assume that a hydrogen monolayer could tie up all of the Si surface dangling bonds and thereby seriously inhibit adsorption of other species such as O. Low-energy electron energy loss spectroscopy could possibly be used to detect the presence of H through the characteristic vibrations of Si-H surface bonds; however, we do not have LEELS capability in our vacuum chamber.

Having developed a method for obtaining very clean Si surfaces without in situ cleaning, we attempted to conduct SPE on such a surface. A 1000-Å amorphous Si film was deposited onto a 2-in. wafer that had no detectable C and less than 50% monolayer of O. SPE growth was conducted at about 600°C since it was anticipated that the growth rate would be lower than for a clean sample.[31] LEED from the surface of the crystallized film exhibited a 2x1 diffraction pattern with weak 1/2-order spots, plus what appeared to be facet spots. Subsequent TEM analysis confirmed that the layer was basically epitaxial but contained a high density of microtwins and dislocation loops. A micrograph showing this high density of defects is presented in Figure 28. Visual examination

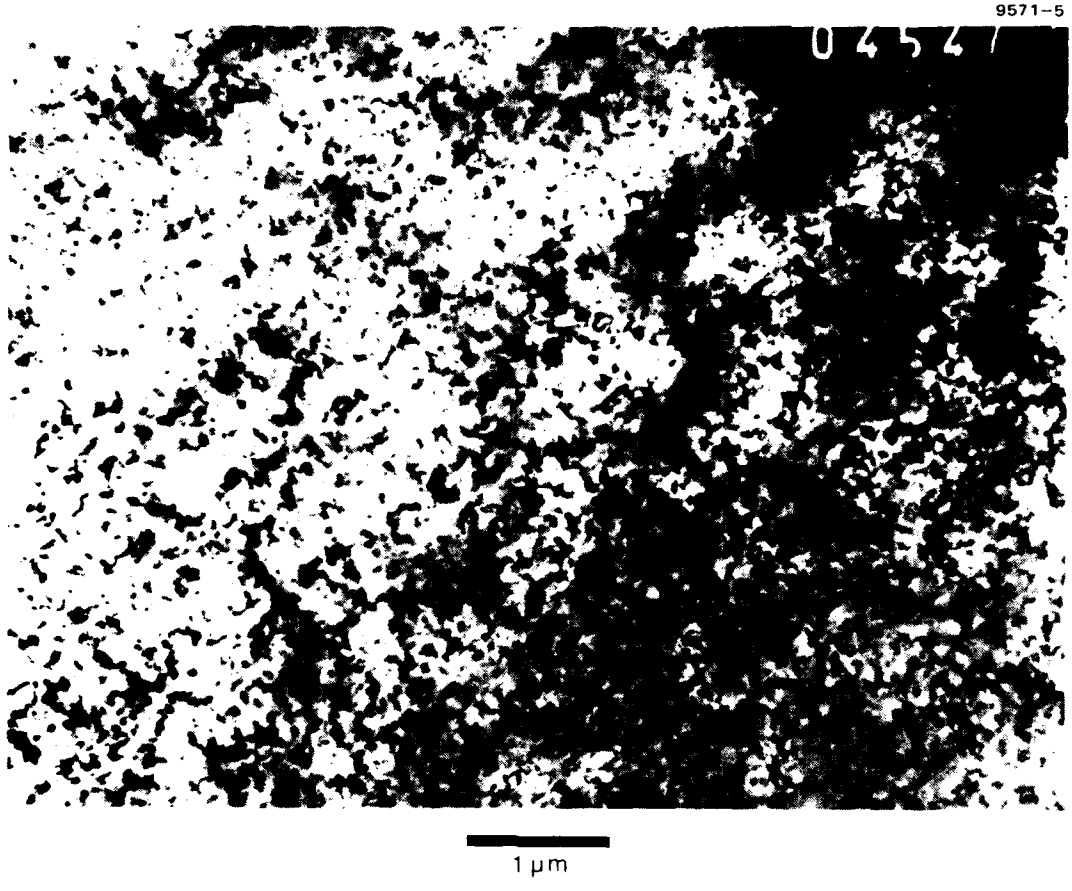


Figure 28. Bright-field TEM micrograph of an SPE Si film grown on a substrate that was not cleaned in the UHV chamber.

of the surface indicated extreme roughness, and this was confirmed by SEM. The micrographs in Figure 29 show three regions of different roughness separated by remarkably well-defined boundaries. Magnified views of the three regions show that, in the rougher areas, the surface features are comparable in size to the thickness of the original film. This suggests that macroscopic transport of Si occurred during heating, which is rather surprising since the growth temperature was only 600°C. In comparison, SPE films grown on atomically clean substrates never exhibit roughness observable in the SEM, so the roughness must be associated with the presence of substrate contaminants. An interesting possibility, which could be checked by high-resolution Auger imaging of O, is that the amplitude of roughness may be governed by the local coverage of contaminants. Thus, patterns of varying roughness in SPE films may reflect the distribution of contaminants on the surface of a chemically cleaned wafer.

Another example of the effect of substrate preparation on SPE was obtained in experiments in which we used only sputter cleaning without subsequent annealing prior to amorphous Si deposition. We know from LEED and Auger analyses that such a surface is disordered and contains a few percent Ar embedded to a depth of 30 Å or less. The Ar is evidently tightly bound since heating to over 750°C is required for its expulsion. One would expect, therefore, that a sputtered but unannealed surface would be a poor template for SPE. Our findings bear this out: after heating a 1000-Å amorphous Si film on such a substrate, the color of the film changed from silver to dark, and could easily be distinguished from the single-crystal substrate, indicating that it was not totally epitaxial.

RBS channeling spectra, presented in Figure 30, suggest that only about 10% of a film grown on sputtered-but-not-annealed Si contains epitaxial columns which reach the surface — the remainder is probably polycrystalline. Thus, the darker color observed is probably due to the small-scale roughness associated with polycrystallite formation. Similar behavior has been seen in annealing of high-dose Ar implants in Si,[34] where the Ar is initially distributed throughout the volume but

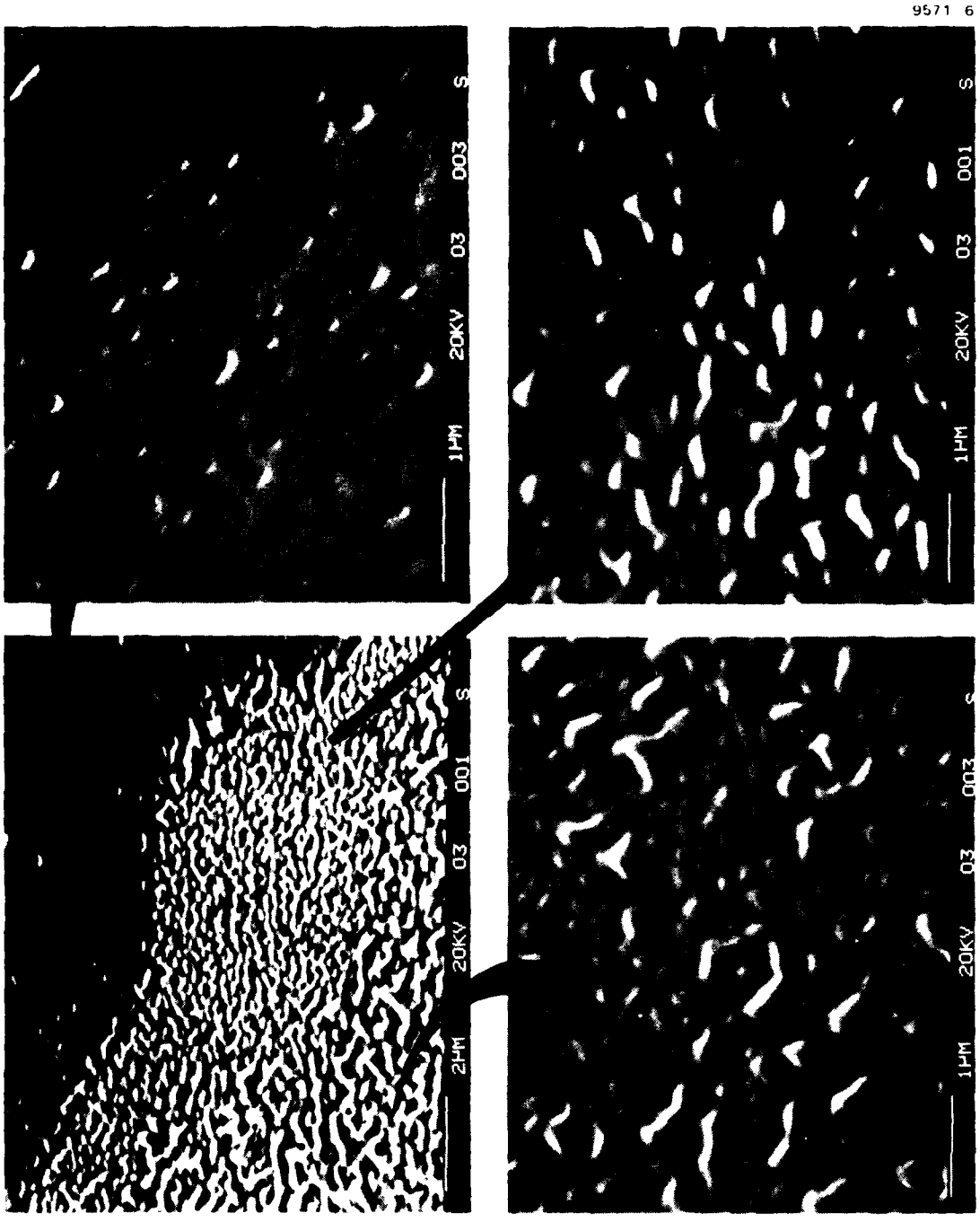


Figure 29. SEM micrographs showing roughness of SPE film grown on a substrate that was not cleaned in the CHV chamber.

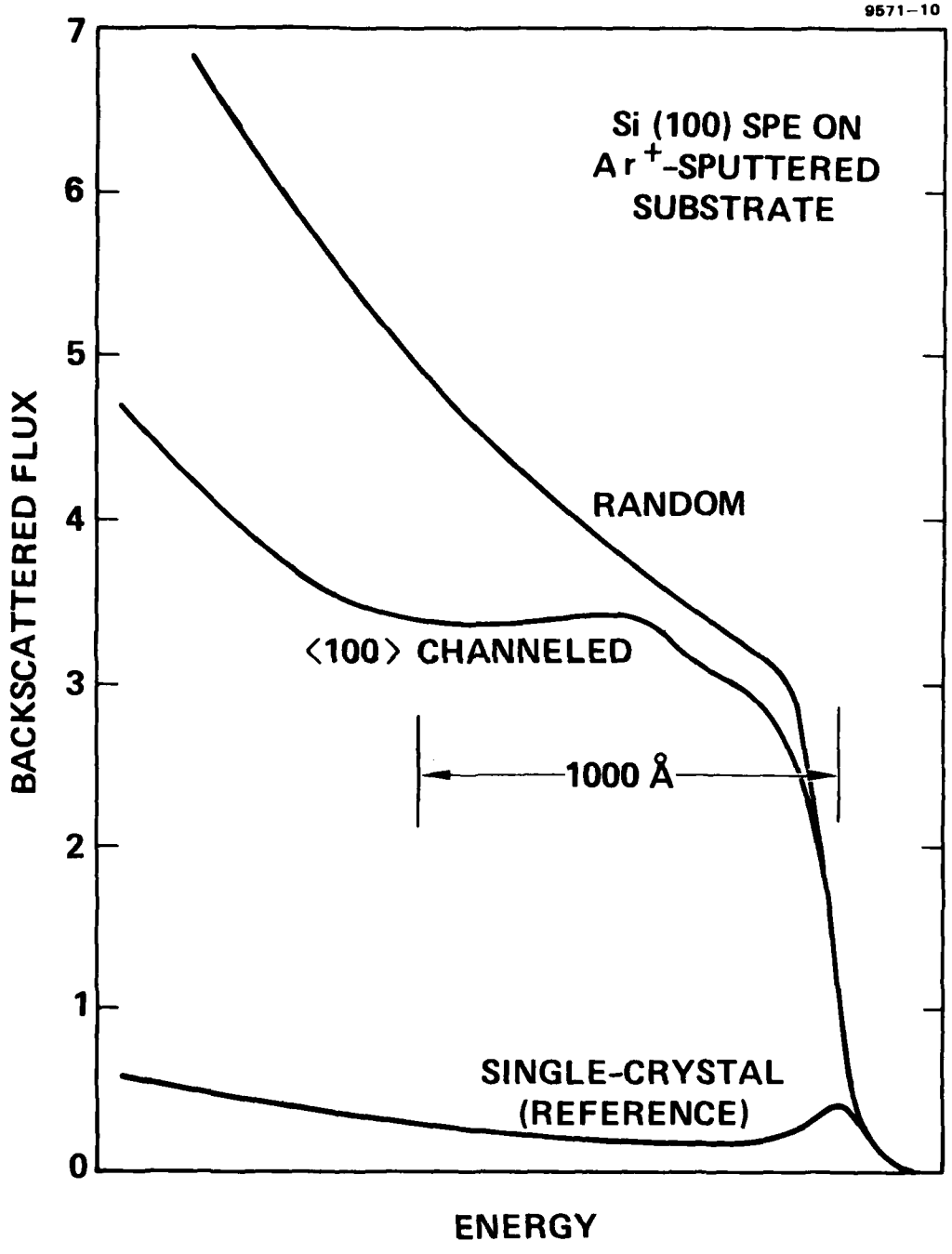


Figure 30. RBS channeling spectra showing the high defect density in an SPE film grown on a substrate not annealed after sputter-cleaning.

coagulates into bubbles during heating. Apparently, the distributed Ar slows SPE growth[26] and the bubbles enhance random nucleation. In our deposited films, the Ar is initially contained in a very thin layer and probably does not redistribute during 550°C heating. Therefore, its effect is probably more like that of substrate contaminants (i.e., the lack of a good template inhibits SPE growth and thereby permits random nucleation to occur throughout the amorphous film). However, epitaxy evidently is able to start in a few areas where either the initial Ar concentration is lower or it is reduced through the coagulation of Ar into interfacial bubbles similar to the volume bubbles observed in the implanted Ar case.

One implication of these findings is that Ar sputtering alone, without subsequent annealing, cannot be used as a cleaning procedure prior to SPE if high-quality films are required. Similarly, the use of sputter-deposition of Si is not recommended due to the possibility of Ar implantation into the substrate and Ar incorporation into the amorphous film.

Numerous experiments on SPE of ion-implanted layers have been conducted successfully using vacuum furnace annealing. Therefore, we also sought to use furnace annealing for deposited films since that would have circumvented the problem of temperature determination in UHV, permitting the growth kinetics to be studied. We immediately noticed, however, that samples prepared in UHV, then removed and transferred to a vacuum furnace, grew more slowly than their UHV-processed counterparts and sometimes failed to change color after annealing. Since we have firmly established that our films do not contain contaminants detectable by AES prior to their removal from the UHV chamber, we investigated the possibility of contaminant introduction during exposure to room air to explain the unusual growth behavior observed.

Figure 31 contains RBS channeling spectra from two 1000-Å-thick films prepared in UHV in different runs and removed to a vacuum furnace for annealing at 550°C. Both samples were heated at least 10 times longer than would be required to completely crystallize an uncontaminated film of comparable thickness. Clearly, there is a vast difference

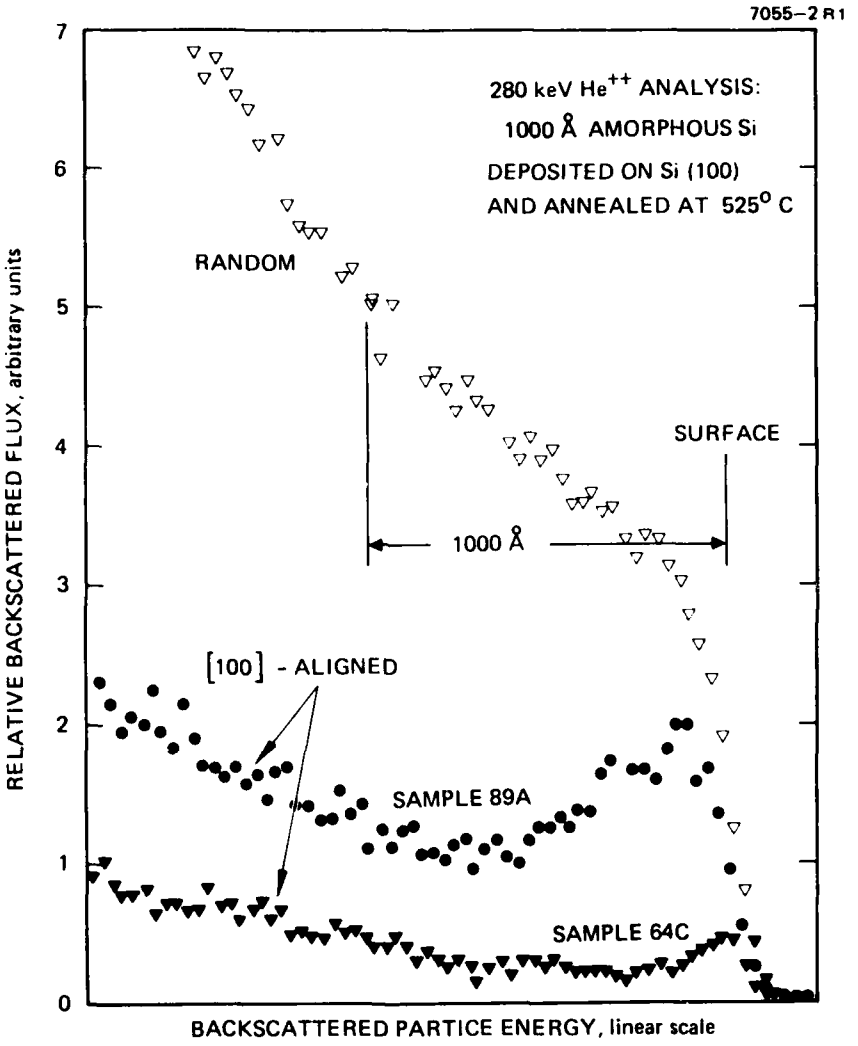


Figure 31. RBS channeling spectra comparing two SPE samples grown in a vacuum furnace at different times.

in the final state of the two samples. Whereas sample 64C grew nearly completely and has a channeling dip comparable to UHV-grown films, 89A only grew epitaxially for a few hundred Å and the remainder of the film became polycrystalline. In the spectrum, the transition from single-crystal yield to random yield is gradual, suggesting that the epitaxial part of the film has protuberances or bumps that extend into the polycrystalline region.

Further examination of the channeling spectrum of sample 64C and other furnace-annealed specimens showed that a polycrystalline surface layer is always formed, which causes the minimum RBS channeling yield, χ_{min}, to be greater than that of UHV-grown films. Moreover, the thickness of the poly layer depends on the initial amorphous Si thickness and is much greater after high-temperature annealing. In Figure 32, the thickness dependence is illustrated by channeling spectra from three films on the same substrate that had been irradiated by a scanned cw laser to produce a growth temperature of ∿1025°C. For each spectrum, the shaded area under the disorder peak was converted to atoms/cm^2 using the known experimental geometry. Thicknesses were calculated from the atoms/cm^2 and the density of single-crystal Si (2.33 g/cm^3).

It is instructive to plot the thickness of epitaxial film grown before poly formation takes over (i.e., the initial film thickness minus the poly layer thickness) versus the initial film thickness. Figure 33 contains such a plot for air-exposed samples grown at normal SPE temperature (550°C) and at high temperature (∿1025°C). Since at 1025°C the epi thickness appears to saturate at around 1000 Å, to grow thicker layers than this requires using lower temperatures. At 550°C, poly formation is minimal, but we must be concerned that air-exposed films may suffer other effects due to contaminant penetration. Indeed, as shown below, all air-exposed amorphous Si films are penetrated to a large extent by atmospheric contaminants.

Table 5 summarizes our results on SPE of deposited films and ion-amorphous layers. In all cases where air exposure was complete epitaxy was obtained and channeling yields were indicative of crystallinity. In contrast, when deposited films were

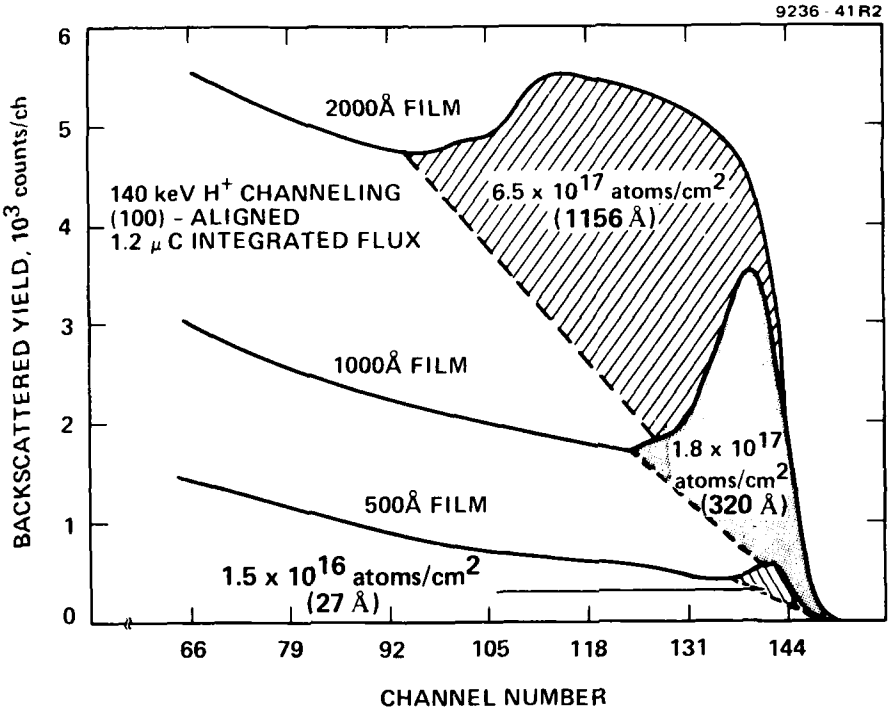


Figure 32. Channeling spectra showing the disordered surface layer on SPE films of three thicknesses grown at 1025°C after exposure to room air.

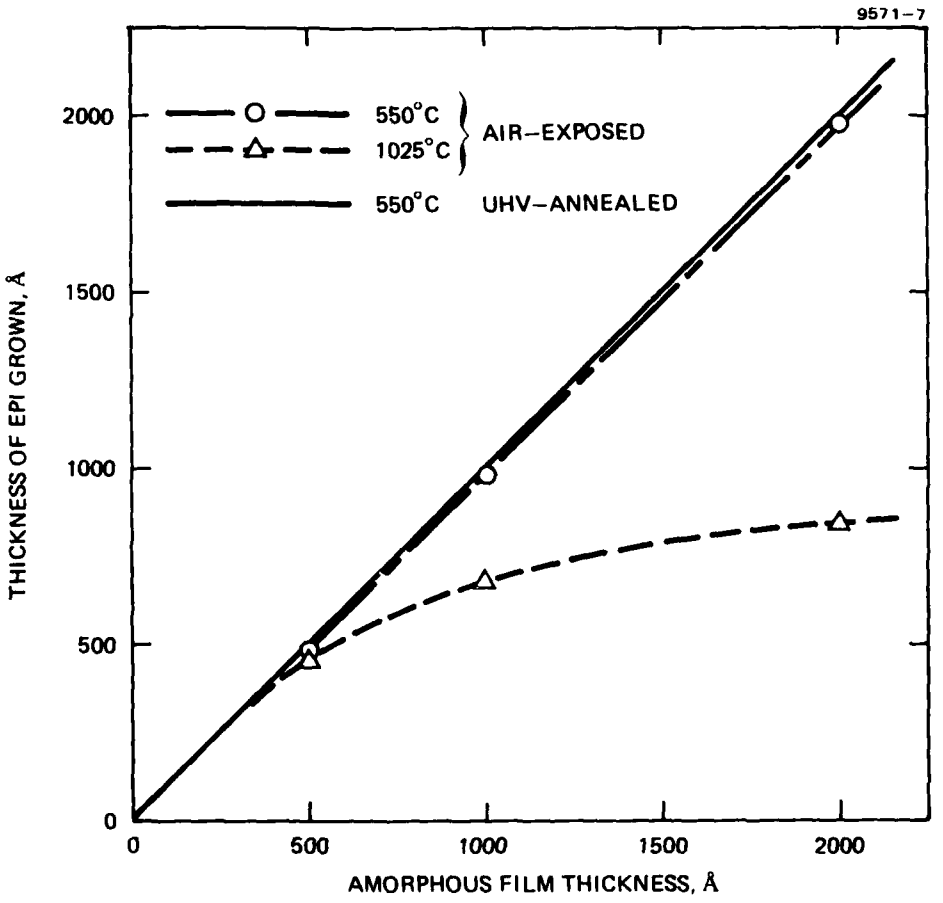


Figure 33. Thickness of the epitaxial (nonpolycrystalline) portion of SPE films grown with and without exposure to room air.

Table 5. Summary of Minimum Channeling Yields, χ_{min}, Measured on UHV-Deposited Films and Ion-Implanted Layers Crystallized by SPE

9571-3

FILM THICKNESS \ ANNEALING METHOD		UHV, RADIANT HEATER (550°C)	HV FURNACE (550°C)	UHV, SCANNED CW LASER (~ 1025°C)	AIR, SCANNED CW LASER (~ 1025°C)
UHV–DEPOSITED FILMS	500 Å	χ = 4% TOTAL EPI	χ = 4.5% ~ 13 Å POLY	χ = 4% TOTAL EPI	χ = 7.8% ~ 27 Å POLY
	2000 Å	χ = 4% TOTAL EPI	χ = 5% ~ 20 Å POLY	χ = 4% TOTAL EPI	χ = 80% 1156 Å POLY
ION–IMPLANTED LAYERS	500 Å TO 1000 Å	NOT TRIED	χ = 4% TOTAL EPI	χ = 4% TOTAL EPI	χ = 4% TOTAL EPI

exposed to room air prior to growth, as in the case of furnace annealing or laser annealing in air, poly formed on the surface and χ_{min} was degraded. In contrast, implanted layers apparently were not affected by exposure to air. To determine the cause of these differences, we used AES depth profiling to obtain concentration profiles of contaminants in Si and found evidence for extensive penetration of carbon and oxygen to depths as great as 2000 Å into deposited films. At the same time, the penetration of C and O into ion-implanted layers or single-crystal Si was found to be negligible, explaining the observed immunity of implants to ambient gas effects.

We recorded AES depth-profiles of C and O concentrations in: (1) UHV-deposited amorphous Si films, (2) deposited films removed from UHV and heated to 550°C in a vacuum furnace for several hours to induce SPE, (3) UHV-deposited films laser annealed in room air, (4) self-ion-implanted <100> Si having a 2000 Å amorphous surface layer, and (5) single-crystal <100> Si exposed to room air for several days. An important feature of our analysis was the examination of deposited films both before and after their removal from UHV, permitting an unambiguous identification of the source of impurities.

Most of the deposited films examined in this study were produced by electron-beam evaporation of 1-ppb-pure Si from a polycrystalline source onto <100> Si. Substrates were cleaned chemically and then loaded into a UHV deposition system (base pressure $<10^{-8}$ Pa, deposition pressure $<5 \times 10^{-7}$ Pa). Argon ion sputter etching and thermal annealing were used to obtain an atomically ordered surface free of contaminants to less than 0.001 monolayer (as judged by AES). Si was deposited onto the unheated substrates at about 1 Å/sec to various total thicknesses, ranging from 500 Å to 2000 Å. The possibility that deposition conditions (i.e., rate, vacuum, temperature) might affect the film microstructure, and thus indirectly affect the extent of contaminant penetration, was addressed by comparing the 1 Å/sec films with amorphous films deposited at higher rates (14 Å/sec and 35 Å/sec) in a different vacuum system (deposition pressure $<7 \times 10^{-5}$ Pa).

Auger spectra were generated with a single-pass CMA using electron-beam excitation at 3 kV and 25 μA into a 500-μm-diameter spot. Depth concentration profiles were produced by progressively ion etching the surface with a 2-keV Ar^+ beam rastered over the Auger excitation spot. Ion current was regulated to produce a 20-Å/sec etch rate. Even though the main ion pump was off during depth-profiling, the partial pressure of gases other than Ar never exceeded 7×10^{-7} Pa. This ensured that the detected C and O Auger signals arose from actual film constituents rather than from gases adsorbed from the vacuum ambient during analysis.

Conversion of the measured dN/dE Auger signals into atomic concentrations was accomplished by using the standard Auger sensitivities published by Davis.[35] For comparison, we also prepared standards for C and O in Si by ion-implanting high doses of these species into separate wafers. Quantities of C and O calculated using the implant standards were about 2.5 and 10 times greater, respectively, then those based on the published sensitivity values.

Depth profiles of oxygen in four types of Si samples are presented in Figure 34. All specimens had a thin oxide surface layer, which caused an O concentration peak to appear in the first 30 Å of the profile. The single-crystal wafer and the implanted specimen exhibit a slight "foot" on their O profiles, which may be due to knock-on or recoil implantation of O from the surface oxide. Nevertheless, the crystal and implanted samples are free of detectable O after sputter-etch removal of about 100 Å of material.

In contrast, the deposited films contain O at levels above 0.08%, well beyond the surface oxide region. (It is important to note that the UHV-deposited film did not contain measurable O before being removed from the vacuum system.) The film deposited at 1 Å/sec has measurable O more than 1000 Å below its surface and reaching nearly to the film/substrate interface. The film deposited at a higher rate contains considerably less absorbed O but still much more than the implanted sample.

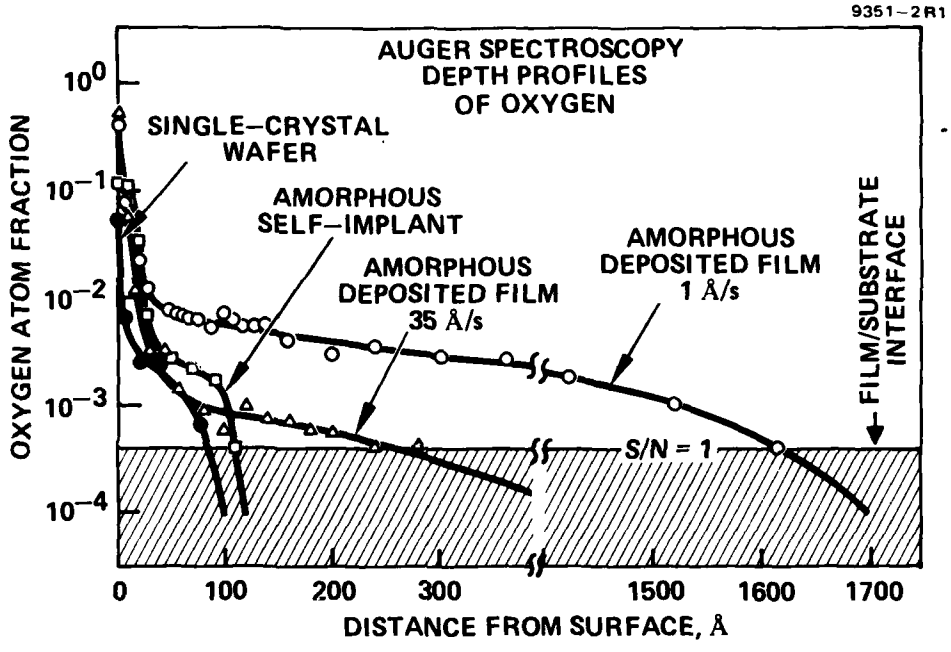


Figure 34. Auger depth profiles of oxygen in UHV-deposited and ion-implanted amorphous Si films exposed to room air.

Carbon concentration profiles presented in Figure 35 show much the same behavior. Carbon does not penetrate as extensively as O in the UHV-deposited, 1-Å/sec film but is comparable to O in the 35-Å/sec samples. Because of the possibility of knock-on during analysis, it is difficult to tell if the apparent higher concentration of C near the surface of the 35 Å/sec film is real or not. Nevertheless, the main conclusion is that C, like O, penetrates into deposited amorphous Si films to macroscopic depths and in large concentrations. (The amorphous self-implant has the thickest layer of adsorbed hydrocarbons on its surface, due to cracking of pump oil on the surface during implantation.)

We could not find a significant difference between O and C concentrations in samples of deposited Si left in the room air only 60 min and those exposed for 30 days. This suggests that the majority of penetration occurs very rapidly, even though the samples are at room temperature. Also, we find that subsequent heating to 550°C does not significantly alter either the distribution or concentration of the contaminant. Thus, it appears that, although the initial penetration of O and C into a deposited amorphous Si film is remarkably rapid, the impurity atoms are bound relatively tightly. Even laser annealing at over 1000°C did not significantly alter the impurity distributions.

The results presented so far can be summarized as follows: (1) deposited amorphous Si films are rapidly penetrated by O and C upon exposure to room air at standard temperature and pressure; (2) the extent of penetration is affected by the film deposition rate; and (3) amorphous Si produced by Si ion-implantation damage is immune to contaminant penetration, or at least suffers far less penetration than deposited films. These observations can be rationalized by noting that there is considerable evidence for a characteristic microstructure in deposited films, namely, they contain low density regions or "voids."[16,17] Dirks and Leamy[18] have recently reviewed the literature on this subject and have shown how voids can arise from self-shadowing of the substrate by atoms of the film. The only prerequisite for obtaining void formation is that atoms of the film have limited mobility (i.e., if they stay fairly close to the location they initially

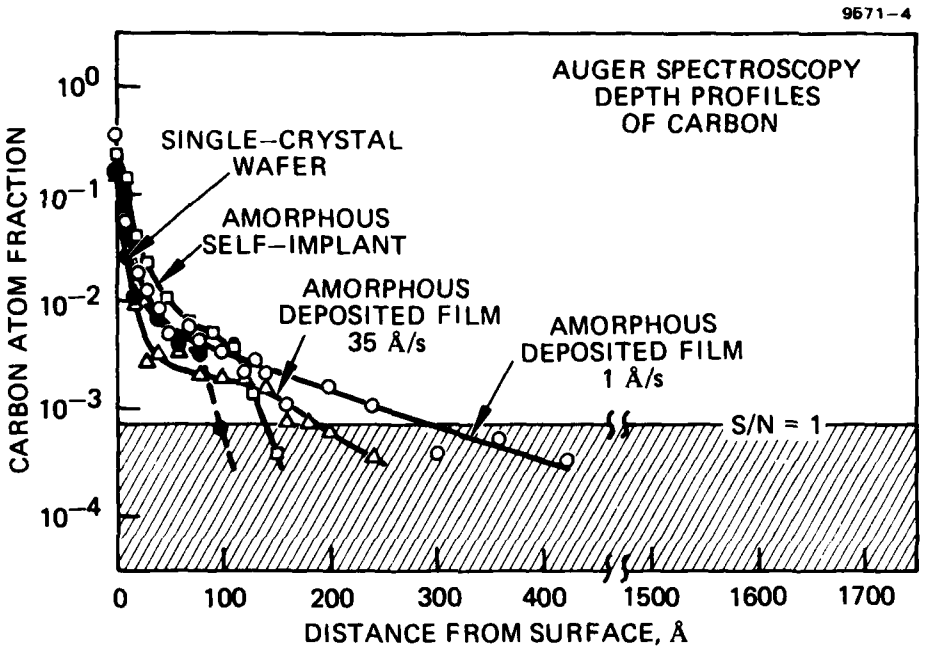


Figure 35. Auger depth profiles of carbon in UHV-deposited and ion-implanted amorphous Si films exposed to room air.

land on). According to computer simulations[18], the fractional volume occupied by voids and their degree of interconnection should depend on the atom mobility within the film. Thus, any factor that can increase the mobility should decrease the number and/or connectedness of voids.

We hypothesize that the contaminant penetration of deposited Si films which we have observed is the result of the presence of an interconnected network of voids in the films. Since the concentration of contaminants does not appear to depend on the duration of exposure to air, we infer that the entire internal void surface is rapidly saturated with foreign atoms which then block further penetration. Apparently, films deposited at a higher rate either have fewer voids or the voids are not as completely interconnected as in slowly deposited films. Implanted layers do not suffer penetration because they are formed by an entirely different process and do not contain voids.

Within this framework, we now suggest a model for the formation of polycrystalline surface layers in SPE of deposited films exposed to air before annealing. As indicated schematically in Figure 36, O and C penetrate into the film through the void network. The primary effect of these contaminants is probably to reduce the growth rate of SPE; this finding is analogous to that of Kennedy et al.[26] on SPE in contaminated implanted layers. Since the concentration of impurities increases toward the film surface (cf. Figure 34), the crystal/amorphous interface does not progress as far during the second interval of heating, τ, as in the first. Because of the slowing of SPE, the imbalance of growth kinetics which normally favors SPE over random nucleation of poly-crystallites is altered, permitting some nuclei to form within the still amorphous portion of the film. These nuclei grow in size and more form as the interface velocity slows still further. If the film is thick enough, and the impurity concentration large enough, the polycrystalline grains can grow together in the outer part of the layer and block further epitaxial crystallization.

The dependence of poly thickness on initial film thickness, presented in Figure 32, is understandable within the framework of this

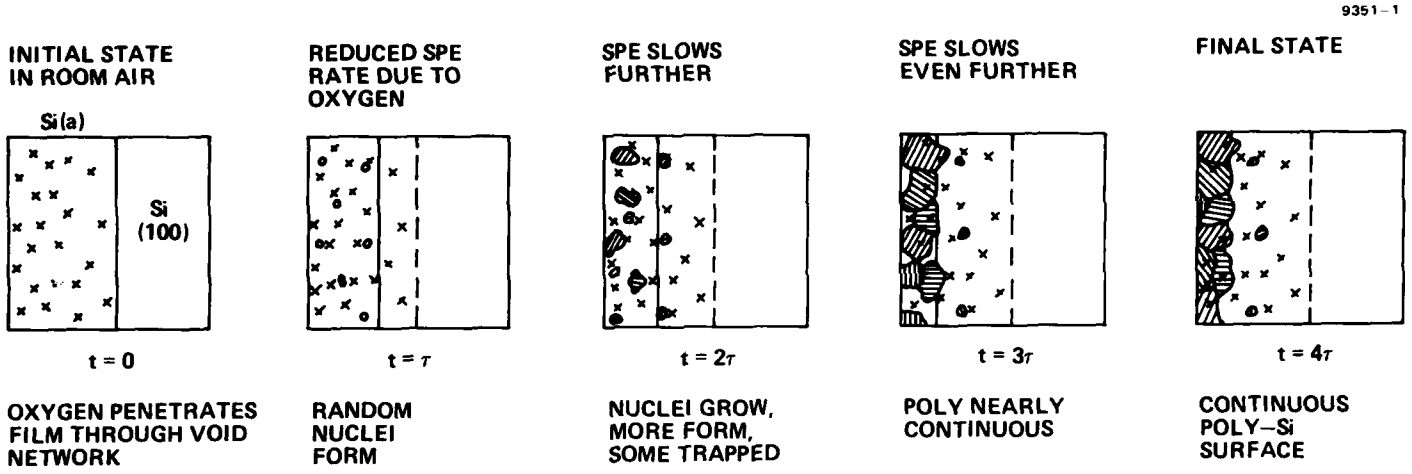


Figure 36. Model for formation of polycrystalline surrace layer in SPE films exposed to air prior to growth.

model. In a thicker film, it takes longer for the crystal/amorphous interface to reach the surface. Therefore, the number and size of random crystallites formed there will be greater. This effect is amplified by the progressive reduction in SPE rate as the growth interface moves into more heavily contaminated material. The growth temperature dependence of poly formation in SPE of deposited films may arise from the faster increase of the rate of amorphous-to-polycrystalline conversion with temperature than the rate of epitaxy. Heterogeneous nucleation at impurity-laden voids may also play a role, but the data presently available are insufficient to address this issue.

SECTION 5

CONCLUSIONS AND RECOMMENDATIONS

We have shown that solid-phase epitaxy occurs in deposited films of Si as well as in implanted layers. Thus, it is now clear that SPE is an intrinsic process that is driven only by the lowering of free energy. The amorphous-to-single-crystal conversion of deposited films by SPE appears to be a very general phenomenon, having now been observed not only in Si[36] but also in Ge on GaAs[37] and in GaAs on GaAs.[1] SPE will probably also soon be extended to the growth of Si on insulators, such as sapphire (SOS), providing a low-temperature alternative growth technology to the standard CVD process currently used for SOS. Growth on other, less chemically stable substrates should also be possible because of the low temperatures used in SPE, thus opening up a wide range of possible substrate/film combinations not previously feasible with high-temperature processing.

Technologically, the most significant aspect of our work is the demonstration that high-quality epitaxial films of Si can be grown by directly depositing Si onto single-crystal substrates, provided that the substrate is properly cleaned in situ. This discovery eliminated the need for metal or silicide interlayers, thus permitting for the first time the growth of high-purity layers usable for microelectronic device fabrication. Moreover, the use of metallic interlayers in SPE was shown actually to be dependent on the presence of contaminants for its successful operation and thus to be intrinsically incapable of producing high-quality epitaxial layers.

In comparison with other forms of Si epitaxy, such as LPE and CVD, growth by SPE has many advantages because it is a low-temperature process. Epitaxial layers can be grown on substrates that have already been partially processed and that contain, for example, complete transistors with their associated oxide and metalization layers. We have successfully used SPE to grow epitaxial Si within openings in a photolithographically defined thermal oxide, thus paving the way for the eventual use of SPE in fabricating transistors having buried oxide and buried interconnect structures. The only requirement is that the substrate must withstand the brief heating to 850°C used to anneal sputter-cleaning damage prior

to Si deposition. The use of refractory metalization layers easily satisfies this requirement.

Another virtue of SPE is that, because the growth temperature is low, dopant atoms do not diffuse measurably during growth. Thus, an undoped or lightly doped SPE layer can be grown on a heavily doped substrate without the substrate dopant penetrating into the epitaxial film. Similarly, dopants within the film do not redistribute during growth, permitting arbitrarily sharp or varying doping profiles to be produced. The ability of SPE to grow thin layers with sharp doping profiles gives it immediate application in the fabrication of high-frequency devices such as IMPATTs and switching transistors. The generation of abrupt emitter/base junctions in bipolar transistors is another potential application of the doping control capability of SPE.

In spite of the low growth temperature employed in SPE, dopants are activated efficiently. Dopant atoms incorporated into the amorphous film attain substitutional sites along with the host atoms during the amorphous-to-crystalline transition. This behavior is consistent with the findings of Tsai and Streetman, who reported very high activation efficiencies for ion-implanted amorphous layers recrystallized by SPE.[38,39] We do not presently know whether the activation efficiency varies with growth temperature for deposited films, but it seems unlikely in view of the results on laser annealing of implanted layers[40] where no temperature dependence is seen.

Although we have fabricated MOS transistors in SPE Si that functioned identically to their bulk Si counterparts, there are other electrical properties that remain to be evaluated before SPE can be considered useful for all microelectronic applications. Bipolar transistors, for example, are more sensitive to certain properties (such as minority carrier lifetime) than are MOS devices, and so it is desirable to fabricate and test bipolar devices. The possibility of deep levels and traps associated with impurity-defect complexes, for example, should be examined by DLTS or photoluminesence spectroscopy. We know that the layers grown to date contain high concentrations of dislocations, but it has not been established whether they will adversely affect the

AD-A084 175 HUGHES RESEARCH LABS MALIBU CA F/G 7/4
SOLID-PHASE EPITAXIAL GROWTH.(U)
APR 80 J ROTH N00014-75-C-0957
UNCLASSIFIED NL

2 OF 2
AD
A084 175

END
DATE FILMED
6-80
DTIC

electrical behavior of devices built in SPE material. Moreover, since most of the defects seen in SPE films appear to be associated with generation sites near the original film/substrate interface, they probably can be eliminated or at least minimized by optimizing the in situ substrate preparation. It also seems reasonable to assume that some of the very small defects seen in TEM may be remnants of the voids present in the initally deposited film. Therefore, changes in the processing schedule that reduce the number of voids or the degree of interconnection of voids would be expected to reduce the SPE defect density accordingly.

Our studies of the effects of contaminants on direct (Si/Si) SPE have shown that, although SPE is an intrinsic process, kinetic considerations are crucial in determining whether a particular amorphous film will become single crystalline or polycrystalline when heated. We have shown that, since the polycrystalline state is very close in free energy to the single-crystal state, modification of the SPE growth rate by contaminants can drastically alter the outcome of the process. A clear indication of competition between amorphous-to-single-crystal and amorphous-to-polycrystal conversion occurs in the SPE of samples containing low-level contamination at the substrate/film interface. Although epitaxial growth is possible in this case, it may be slowed sufficiently to permit an amorphous-to-polycrystalline transition to occur in the outer portions of the film before the crystal/amorphous interface reaches the surface. Similarly, in SPE of films deposited onto <111>-oriented Si, the epitaxial growth rate is evidently so much lower than on <100> substrates that gross poly formation occurs even in uncontaminated samples.

If the amorphous film is extremely thick, the outermost portions may undergo random nucleation before the growth interface arrives. This in effect establishes a practical upper limit on epitaxial layer thickness for SPE without poly formation. Our results on laser-annealed SPE show that the maximum thickness is less at high growth temperatures, but it is not yet possible to specify the limit precisely because our knowledge of the crystallization kinetics is imperfect.

Ideally, one would like to calculate the density of random nuclei formed in SPE as a function of thickness and growth temperature. To do this would require greatly improved data on the kinetics of the amorphous-to-polycrystalline transition in deposited films. Previous crystallization rate measurements[29,30] performed under conditions we now know would have resulted in serious contaminant penetration of the amorphous films are probably not applicable to clean specimens. Moreover, since past measurements were limited to temperatures below about 650°C, there is presently no rational basis for extrapolation into the high-temperature regime now being explored in laser-induced SPE experments.[28,40] Consequently, we cannot yet say whether there is an optimum growth temperature with regard to defect density in SPE.

A fundamental problem in extending the temperature range of data on crystallization kinetics is the difficulty of rapidly establishing the actual growth temperature and accurately measuring it. However, with the advent of carefully controlled scanning-laser irradiation systems and our recent coupling of laser heating with a UHV annealing ambient,[28] there is reason to believe that accurate kinetic data can eventually be obtained in the high-temperature regime. In the future, this will permit a sensible evaluation of the tradeoff between the time required to grow an SPE layer and the resulting quality of the film.

In summary, we have shown that high-quality epitaxial layers of Si can be grown at low temperatures, provided that the introduction of impurities is strictly avoided. The process is relatively simple but requires ultra-high-vacuum processing for the growth of device-quality films. The combination of low growth temperature, implicit thickness control, and the ability to incorporate any desired doping profile makes solid-phase epitaxy an attractive alternative to chemical vapor deposition for the production of substrates for sophisticated microelectronic devices of the future.

REFERENCES

1. A.Y. Cho, Surf. Sci. 17,494 (1969).

2. F. Jona, "Surfaces and Interfaces," edited by J.J. Burke, N.C. Reed, and V. Weiss (Syracuse U.P., Syracuse, N.Y. 1967).

3. S.S. Lau, Caltech, private communication.

4. A. Christou, J.E. Davey, H.M. Day, and H.B. Dietrich, Appl. Phys. Lett. 30, 598 (1977).

5. C. Canali, J.W. Mayer, G. Ottaviani, D. Sigurd, and W. Van der Weg, Appl. Phys. Lett. 25, 3 (1974).

6. Z.L. Liau, S.S. Lau, M-A. Nicolet, J.W. Mayer, R.J. Blattner, P. Williams, and C.A. Evans, Jr., Proceedings of the Third International Conference on Ion Beam Analysis, Washington, D.C., 1977, Nucl. Inst. and Meth.

7. Z.L. Liau, private communication.

8. R.C. Henderson, J. Electrochem. Soc. 119, 772 (1972).

9. H. Sankur, J.O. McCaldin, and J. Devaney, Appl. Phys. Lett. 22, 64 (1973).

10. G. Ottaviani, D. Sigurd, V. Marrello, J.W. Mayer, and J.O. McCaldin, J. Appl. Phys. 45, 1730 (1974).

11. J.E. Davey, A. Christou, and H.M. Day, Appl. Phys. Lett. 28, 365 (1976).

12. C. Canali, S.U. Campisano, S.S. Lau, Z.L. Liau, and J.W. Maery, J. Appl. Phys. 46, 2831 (1975).

13. S.S. Lau, Z.L. Liau, M-A. Nicolet, and J.W. Mayer, J. Appl. Phys. 48, 917 (1977).

14. Z.L. Liau, S.U. Campisano, C. Canali, S.S. Lau, and J.W. Mayer, J. Electrochem. Soc. 122, 1696 (1975).

15. R. Pretorius, Z.L. Liau, S.S. Liau, and M-A. Nicolet, Appl. Phys. Lett. 29, 598 (1976).

16. T.M. Donovan and K. Heineman, Phys. Rev. Lett. 27, 1794 (1971).

17. F.L. Galeener, Phys. Rev. Lett. 27, 1716 (1971).

18. A.G. Dirks and H.J. Leamy, Thin Solid Films 47, 219 (1977).

19. S.S. Lau, Caltech, private communication.

20. W.D. Buckley and S.C. Moss, Solid-State Electronics 15, 1331 (1972).

21. J.C. Bean, G.E. Becker, P.M. Petroff, and T.E. Seidel, J. Appl. Phys. 48, 907 (1977).

22. M. Cardillo, talk presented at the Thirty-Fifth Conference on Physical Electronics, University of Maryland, June 18-20, 1979.

23. B.A. Joyce, Rep. Prog. Phys. 37, 363 (1974).

24. L. Csepregi, J.W. Mayer, and T.W. Sigmon, Appl. Phys. Lett. 29, 92 (1976).

25. S.S. Lau, Caltech, private communication.

26. E.F. Kennedy, L. Csepregi, J.W. Mayer, and T.W. Sigmon, J. Appl. Phys. 48, 4241 (1977).

27. L. Csepregi, J.W. Mayer, and T.W. Sigmon, Phys. Lett. 54A, 157 (1975).

28. L.D. Hess, J.A. Roth, G.L. Olson, H.L. Dunlap, V. vonAllmen, and J. Peng, in Proceedings of the Symposium on Laser and Electron Beam Processing of Materials, Boston, MA Nov. 1979 (AIP Press, New York, NY 1980), in press.

29. N.A. Blum and C. Feldman, J. Non-Cryst. Sol. 11, 242 (1972).

30. U. Koster, Phys. Stat. Sol. A48, 313 (1978).

31. M. von Allmen, S.S. Lau, J.W. Mayer, and W.F. Tseng, Appl. Phys. Lett. 35, 280 (1979).

32. S.I. Raider, R. Flitsch, and M.J. Palmer, J. Electrochem. Soc. 122, 413 (1975).

33. H. Ibach and J.E. Rowe, Surf. Sci. 34, 809 (1975).

34. B.Y. Tsaur, Z.L. Liau, J.W. Mayer, and T.T. Sheng, J. Appl. Phys. 50, 3978 (1979).

35. L.E. Davis et. al., "Handbook of Auger Electron Spectroscopy," p. 13 (Physical Electronics Division, Perkin-Elver Corporation, Eden Prairie, Minn., 1978).

36. J.A. Roth and C.L. Anderson, Appl. Phys. Lett. 31, 689 (1977).

37. J.A. Roth, unpublished.

38. B.L. Crowder, J. Electrochem. Soc. 118, 943 (1971).

39. M.Y. Tsai, B.G. Streetman, V.R. Deline, and C.A. Evans, Jr., J. Electronic Mater. 8, 111 (1979).

40. L.D. Hess, J.A. Roth, C.L. Anderson, and H.L. Dunlap, in Laser-Solid Interactions and Laser Processing — 1978, edited by S.D. Ferris, H.J. Leamy, and J.M. Poate, (American Institutes of Physics, New York, 1979) pp. 496-502.

SUPPLEMENTARY DISTRIBUTION LIST FOR REPORTS GENERATED
UNDER CONTRACT NUMBER N00014-75-C-0957 WITH THE OFFICE OF NAVAL RESEARCH

Professor M. A. Littlejohn
North Carolina State University
Electrical Engineering Department
Raleigh, North Carolina 27607

Professor W. Gibson
State University of New York
Department of Physics
Albany, New York 12222

Professor James W. Mayer
California Institute of Technology
Electrical Engineering Department
Pasadena, California 91109

Dr. Marc-A. Nicolet
California Institute of Technology
Electrical Engineering Department
Pasadena, California 91125

Dr. J. Comas
Naval Research Laboratory
Code 6812
4555 Overlook Avenue, S.W.
Washington, D.C. 20375

Professor J. O. McCaldin
California Institute of Technology
Department of Applied Physics
Pasadena, California 91125

Dr. B. McCombe
Naval Research Laboratory
Code 5270
4555 Overlook Avenue, S.W.
Washington, D.C. 20375

Dr. John Davey
Naval Research Laboratory
Code 5210
4555 Overlook Avenue, S.W.
Washington, D.C. 20375

Dr. R. M. Walser
The University of Texas at Austin
Electronics Research Center
Austin, Texas 78712